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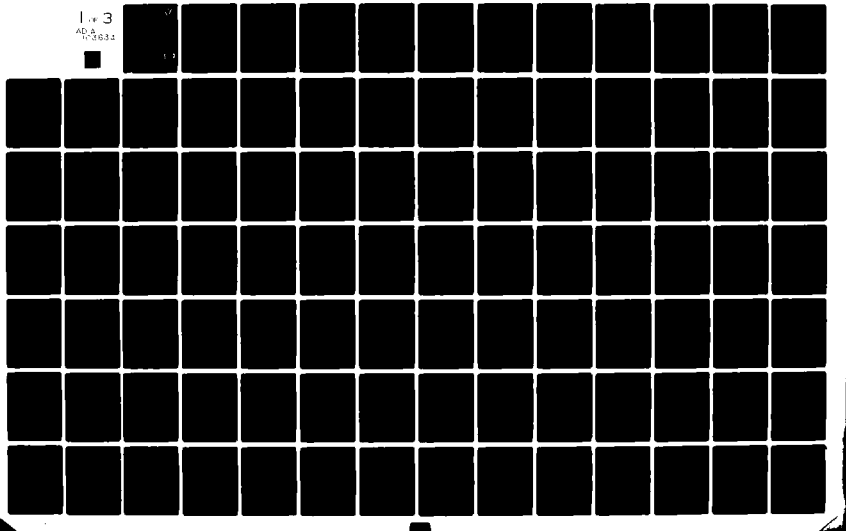

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LEVEL II

CHARGE TRAPPING IN

INTERFACE DOPED MNOS STRUCTURES

DISSERTATION

AFIT/DS/EE/81-2 William G. Sutton
Captain USAF

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MNOS
Charge Centroid
Thermally stimulated current
Nonvolatile semiconductor memory
Interface doped MNOS
Metal-Nitride-Oxide-Semiconductor
Semiconductor memory device

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Evaporated tungsten interface dopant, oxide-nitride interface and nitride bulk traps in MNOS structures were examined using charge centroid and thermally stimulated current (TSC) techniques. Trapping in dopant traps occurred at low injected charge levels. Above a "saturation" level trapping occurred in the nitride, and the charge centroid penetrated into the nitride. TSC measurements were made on MNS, MNOS, and interface doped MNOS devices. Analysis of TSC spectra yielded trap depths for the interface dopant and oxide-nitride interface

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20. ABSTRACT

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of 1.71 - 1.86 and 0.70 - 1.34 eV respectively, and charge densities up to 6×10^{12} cm^{-2} and 3×10^{13} cm^{-2} respectively.

A model of MNOS charging and discharging was developed. Electron charging is by Fowler-Nordheim (F-N) injection from the silicon into the oxide conduction band, trapping at the oxide-nitride interface and Poole-Frenkel (P-F) conduction in the nitride. Discharging occurs by: (1) F-N injection of holes from the silicon into the oxide valence band and recombination with trapped electrons at the oxide-nitride interface and the nitride, and (2) redistribution of trapped electrons toward the silicon via P-F conduction and F-N injection from the nitride into the silicon. Calculated write/erase and charge centroid characteristics were compared with measured data. 105 item bibliography.

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CHARGE TRAPPING IN INTERFACE DOPED MNOS STRUCTURES

DISSERTATION

Presented to the Faculty of the School of Engineering

of the Air Force Institute of Technology

Air University

in Partial Fulfillment of the

Requirements for the Degree of

Doctor of Philosophy

by

William G. Sutton, BSEE, MSEE

Captain USAF

AFIT/DS/EE/81-2

CHARGE TRAPPING IN

INTERFACE DOPED MNOS STRUCTURES

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SYMBOLS

A	Area	102
C_I	Injected charge integrator capacitor	65
$C_{MNOS}(i)$	Total MNOS capacitance at time instant i	56
C_N	Nitride capacitance/area	55
C_{No}	Total oxide/nitride capacitance/area	45
C_o	Oxide capacitance/area	41
DMNOS	Interface Doped MNOS	29
E_c	Energy level, conduction band	39
E_g	Energy bandgap	41
E_f	Energy level, Fermi	39
E_t	Energy level of trap	85
E_v	Energy level, valence band	39
F	Nitride electric field	137
F_i	Electric field in region i, i=1,3	42
F_m	Electric field in metal	43
F_{NO}	Initial nitride electric field	54
F_{ox}	Oxide electric field	54
F_s	Electric field at semiconductor surface	43
h	Planck's constant: 6.625×10^{-35} joule seconds	137
I, I_o, I_i	Current, i=1,3	87
I_{max}, I_m	Current at TSC peak maximum	87
J, J_o	Current density	55
J_N	Current density in nitride at gate	55
k	Boltzmann's constant: 1.38×10^{-23} joule/^oK	85
m^*	Effective mass of carrier	89

MIS	Metal-insulator-semiconductor	38
MNOS	Metal-nitride-oxide-semiconductor	2
MNS	Metal-nitride-semiconductor	4
n_t	Occupied trap charge density	138
N_c	Effective density of states in conduction band	86
N_D	Donor density	40
N_t	Number of TSC released charges	101
N_t	Trap density	141
q	Electron charge: 1.6×10^{-19} coulombs	40
$q_i(t)$	Total charge/area in insulators at time t	55
q_0	Total initial stored charge/area	59
Q	Localized charge/area in nitride	45
Q(t)	Total injected charge/area (Integral of current density)	55
$Q_d; Q_{d,0}$	Depletion layer charge/area; zero bias charge	40
Q_{dmax}	Maximum depletion layer charge/area	42
Q_{eff}	Effective semiconductor surface charge/area	44
Q_g	Charge/area on gate	40
$Q_n; Q_{n,0}$	Inversion layer charge/area; zero bias charge	40
Q_{ox}	Fixed charge/area in oxide	42
Q_p	Charge density of charge "packet"	141
$Q_s; Q_{s,0}$	Total semiconductor charge/area; zero bias charge	40
$Q_s(t)$	Q_{ss} + depletion layer charge/area at time t	55
Q_{ss}	Fixed, semiconductor surface charge/area	40
$Q_T; Q_T(0)$	Total charge/area stored in nitride; initial charge	52
Q/A	Total injected charge/area from centroid measurement	71
RBS	Rutherford Backscattering	Appendix I
t	time	

t_i	Time instants, i=1,3	68
T, T_o, T_i	Temperature, i=1,3	87
T_h	Temperature of TSC peak half max (low temperature side)	85
T_m	Temperature of TSC peak maximum	85
T_N	Nitride thickness	45
T_{ox}	Oxide thickness	41
TSC	Thermally stimulated current	29
v_{th}	Thermal velocity of carrier	86
V_{FB}	Flatband voltage	5
$V_{FB}(t)$	Flatband voltage at time t	58
$V_{FB_I}; V_{FB_\pm}$	Flatband voltage: initial; after + or - write pulse	5
V_g	Gate voltage	14
V_i	Voltage across insulator segment i, i=1,3	49
$V_N; V_{N,0}$	Nitride voltage; zero bias nitride voltage	46
V_{new}	Bias voltage during centroid measurement	56
$V_o; V_{o,0}$	Oxide voltage; zero bias oxide voltage	39
V_{start}	Bias voltage during centroid measurement	56
V_{TH}	Threshold voltage	9
X_c	Nitride charge centroid	52
X_S	Centroid of charge injected from silicon	59
$X_0(t)$	Centroid of initial charge distribution at time t	59
α	Linear heating rate	86
β	Poole-Frenkel constant	89
δ_o	$X_o(t) - X_o(0)$	59
Δn_t	Number of charges in traps	138
$\Delta q_i(t)$	$q_i(t) - q_i(0)$	55

Δt	Time period	138
ΔQ_p	Number of charges trapped from charge packet	141
$\Delta Q_s(t)$	$Q_s(t) - Q_s(0)$	55
ΔV_{bias}	$V_{new} - V_{start}$	56
ΔV_{FB}	Flatband voltage shift during centroid measurement	56
$\Delta V_{FB}(t)$	$V_{FB}(t) - V_{FB}(0)$	58
$\Delta\phi_B$	Image force barrier lowering	138
ε_n	Permittivity of nitride	45
ε_{ox}	Permittivity of oxide	42
ν	Attempt-to-escape frequency	86
$\rho(x)$	Charge distribution in oxide or nitride	44
$\rho(x,t)$	Total charge distribution at time t	58
$\rho_g(x,t)$	Charge distribution injected from gate at time t	58
$\rho_o(x,0)$	Initial stored charge distribution at t=0	58
$\rho_o(x,t)$	Initial stored charge distribution at time t	58
$\rho_s(x,t)$	Charge distribution injected from silicon at time t	58
σ	Capture cross section of trap	86
$\sigma(T_m), \sigma_o$	Conductivity	87
ϕ_B	Energy barrier height	137
ϕ_F	Fermi potential	39
ϕ_m	Metal work function	39
ϕ_{mn}	Metal-nitride energy barrier	46
ϕ_{oxn}	Oxide-nitride energy barrier	46
$\phi_s; \phi_{s,0}$	Semiconductor surface potential; zero bias potential	39
$\phi_s(t)$	Silicon surface potential at time t	55
χ	Semiconductor electron affinity	39

ABSTRACT

Parameters of evaporated tungsten interface dopant induced traps, naturally occurring oxide-nitride interface traps and nitride bulk traps in conventional and interface doped MNOS structures were examined using charge centroid and thermally stimulated current techniques. Charge centroid measurements showed charge trapping in interface doped MNOS structures occurred at the oxide-nitride interface for injected charge levels below a trap "saturation" level. The saturation level depended more on the oxide thickness than on the dopant density, decreasing as oxide thickness increased. Above the saturation level considerable charge trapping in the nitride occurred, causing the charge centroid to approach the mid-point of the nitride. Conventional MNOS structures exhibited charge centroid values equal to the nitride mid-point. Thermally stimulated current measurements were made on MNS, MNOS and interface doped MNOS devices. Comparisons of the spectra from the three types of devices permitted separation of the nitride, the oxide-nitride interface and the interface dopant induced traps. Analysis of the spectra yielded trap depths and trapped charge densities. It was determined that interface dopant traps were 1.71 - 1.86 eV, oxide-nitride interface traps were 0.70 - 0.93 and 1.30 - 1.34 eV and nitride traps were 1.14 - 1.19, 1.35 - 1.58 and 1.92 - 2.32 eV below the nitride conduction band. Detrapped charge densities up to $6 \times 10^{12} cm^{-2}$ from interface dopant traps, $3 \times 10^{13} cm^{-2}$ from oxide-nitride interface traps, $1.5 \times 10^{18} cm^{-3}$ from shallow nitride traps and $8 \times 10^{18} cm^{-3}$ from deep nitride traps were measured.

A model of the charging and discharging processes in MNOS

structures was developed. Positive bias charging is by Fowler-Nordheim injection of electrons from the silicon conduction band into the oxide conduction band, trapping at the oxide-nitride interface and trapping and Poole-Frenkel detrapping throughout the nitride. Negative bias discharging occurs by two mechanisms. There is Fowler-Nordheim injection of holes from the silicon valence band into the oxide valence band and hole trapping and recombination with trapped electrons at the oxide-nitride interface and throughout the nitride. Additionally, trapped electrons undergo redistribution toward the silicon via Poole-Frenkel detrapping and retrapping and Fowler-Nordheim injection from the nitride conduction band into the silicon. This model was verified by comparison of calculated write/erase and charge centroid characteristics with measured data.

1. CHAPTER ONE - INTRODUCTION, BACKGROUND and SUMMARY

1.1 Introduction

There are many applications, both commercial and military, for nonvolatile semiconductor memory elements. Considering avionics there are two prime application areas for nonvolatile memories - in radar signal processors and in guidance and control systems. A single radar signal processor can be adapted to various functions or missions (ie. terrain following or side looking) through the use of electrically alterable read only memories (EAROM). For this use, a long retention time device is required, but the number of write/erase cycles it will undergo would be small since reprogramming of the memory would rarely occur more frequently than weekly. Guidance and control systems require fully random access memories (RAM) for in-flight computations. The RAM must also be nonvolatile under power down conditions which are instituted upon detection of hostile radiation so that the vehicle can continue to target after the radiation threat to electronic circuits is passed. The required retention time in this case is very short, seconds or less, but the memory devices must be capable of undergoing many fast write erase cycles without degradation.

Although most switching and logic applications do not need nonvolatile memories, there are many in which a truly nonvolatile memory element would be a great advantage. Long distance space probes which have on-board, stored program, computers could be totally turned off until arrival at the destination. Although a preprogrammed read-only-memory would satisfy this requirement, an electrically

alterable nonvolatile memory would not only satisfy the requirement but would also have the capability for reprogramming to meet unplanned exigencies. No quiescent power to maintain the state of memory elements need by provided; hence, the total power requirement is reduced. This requires a long retention time device which is also capable of many cycles of operation after activation. At any location where data are received, processed or transmitted, whether manned or unattended, loss of information can occur upon power failure unless the back-up power is continuously on, and on-line. This is expensive. Use of nonvolatile elements precludes the need for on-line back-up power, allowing the use of generators which can be turned on and switched on line after primary power outage has occurred. This requires a memory device capable of many cycles of write/erase operation and short and low voltage write/erase pulses during normal operation, but only a relatively short (seconds to hours) retention time upon power failure.

One form of presently available nonvolatile semiconductor memory is a dual dielectric structure - the metal-nitride-oxide-semiconductor (MNOS) device. The basic principle of this device, appreciable charge storage in the nitride, causes usage problems. The capability for appreciable charge storage for long periods of time totally conflicts with fast, low voltage write/erase signal capability. This prohibits realization of many possible applications for nonvolatile memories.

The interface doped, dual dielectric cell has been offered as a solution to the write/erase-retention problems of charge storage type devices for non-volatile semiconductor memories and as a means to increase the write speed or decrease the write voltage for these

devices. It has been proposed by Kahng et al[1] that the interface doping creates localized charge trapping at the interface of the two dielectrics and thus prevents charge penetration and trapping in the bulk of the outer dielectric layer. A detailed understanding is needed of the charge trapping process in the interface doped dual dielectric cell which Kahng, and more recently Neugebauer,[2, 3] have observed to lead to a two order of magnitude faster write speed for the same memory retention period.

The objective of this work was to develop a model of the charge trapping process in a specific embodiment of the interface doped dual dielectric cell: the interface doped, metal-nitride-oxide-semiconductor (DMNOS) device. This model would describe charge trapping in the device in terms of interface dopant and nitride trap parameters and appropriate tunneling theory. This model could then be used to predict the write/erase and retention characteristics of a device prior to fabrication thus permitting design optimization of characteristics rather than empirical optimization. Experimental data developed in this effort would test Kahng's localized charge trapping proposal and also lead to the first description of the characteristics of the interface dopant traps.

1.2 Background

Historically, the MNOS structure developed out of problems in metal-insulator-semiconductor or metal-oxide-semiconductor (MOS) devices. The MOS structures exhibited a variation in threshold voltage due to drift of ions in the oxide (primarily sodium ion contamination).[4] The ion drift direction depended on the magnitude and polarity of the

gate bias. Additionally, the silicon dioxide density was low enough that it remained permeable to water vapor (residual moisture during or after packaging). Consideration was given at that time to using a denser insulator to slow down the drift action and seal the surface. Tombs et al[5] suggested the use of silicon nitride in place of the silicon dioxide. The density of silicon nitride is 3.44 g/cc while that of silicon dioxide is 2.2 g/cc. Devices with the metal-silicon nitride-silicon (MNS) structure were fabricated. They showed little ion drift problems. Further study of the MNS system[6, 7] pointed out that it exhibited a threshold voltage hysteresis effect which depended on the past history of the amplitude, duration and sign of the gate bias which had been applied to the device. This effect was examined primarily through observation of capacitance-voltage curves. Data showed that as the bias voltage was made more negative the C-V curves (and hence the flatband and threshold voltages) shifted to more negative values. This is shown in Figure 1-1. This occurred for low (less than 10V) bias conditions. This was not desirable for the usual FET applications. The presumption was that the cause was charge trapping at the silicon-silicon nitride interface and in the silicon nitride.

To attempt to eliminate the above problem several ideas were combined.[6] (1) The silicon-silicon dioxide system interface was known to have a low surface state density when proper fabrication care was taken. (2) A thick dense nitride layer would have low ion drift. (3) A thin silicon dioxide layer would display a negligible ion problem. Thus a final structure composed of a silicon substrate, a thin silicon dioxide buffer layer and a thick silicon nitride layer was proposed by Chu et

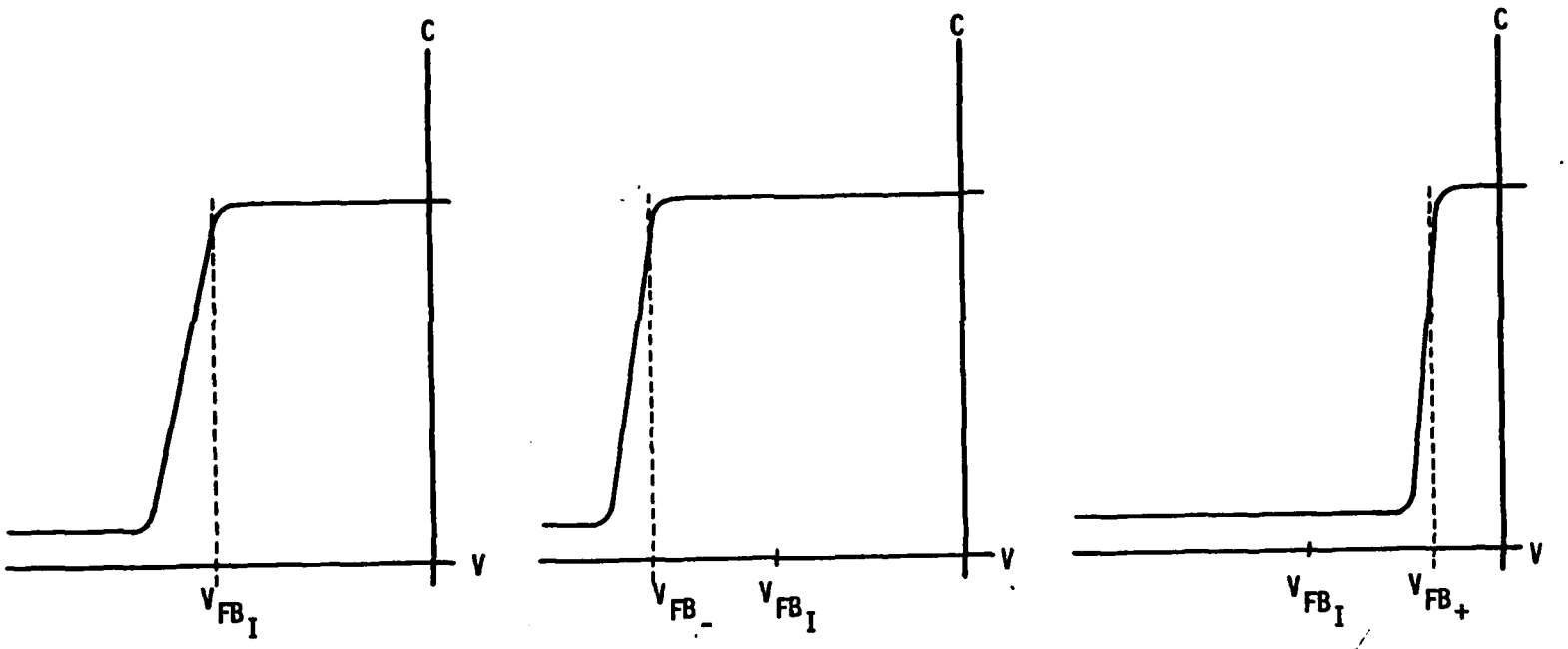


Figure 1-1: Typical MNS and MNOS C-V Curve Shifts

al. (See Figure 1-2 for this structure in FET form and Figure 1-3 for an ideal energy diagram of the MNOS structure.) This structure then had no ionic problems, a low surface state density at the silicon-silicon dioxide interface, and showed no charge trapping hysteresis for moderate bias voltages because the silicon dioxide insulator provided a charge trapping barrier. However, above a critical bias voltage (dependent on SiO_2 thickness) a threshold voltage shift effect was again observed.

Subsequent investigation[8, 9] showed that the MNOS structure, used as an insulated gate field effect transistor (IGFET) gate structure, held the promise of a non-volatile, electrically alterable, non-magnetic memory element. Depending on the device fabrication process, conduction in the oxide layer and in the nitride layer could be made to differ by many orders of magnitude. An appropriate polarity, high magnitude voltage pulse, applied to the metal gate, would cause charge accumulation in the region of the oxide-nitride interface due to the differing conduction in the two insulators. Figure 1-4 shows the energy band conditions and the corresponding C-V curves and field effect transistor threshold voltages for an MNOS structure on an n-type silicon substrate with the condition of a positive charge accumulation at the oxide-nitride interface in Figures 1-4(a) and (c) and the condition of a negative charge accumulation at the oxide-nitride interface in Figures 1-4(b) and (c). Once trapped in the insulator the charges have been shown[10, 11] to undergo a very slow back-tunneling through the oxide and similarly slow redistribution into the nitride when the gate bias is reduced to zero or to the low level used to "read" memory transistors.[11, 12, 13] Hence the charge is "permanent" and the

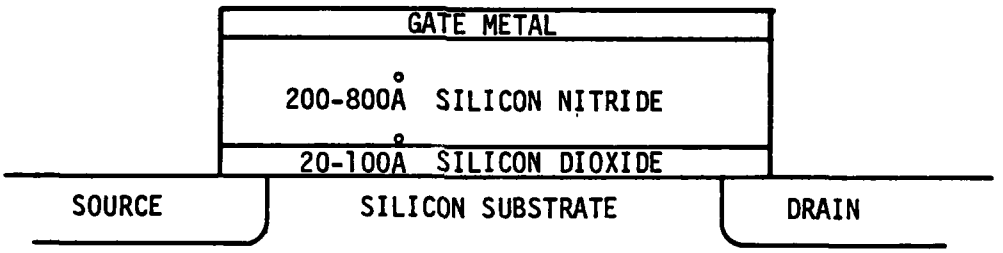


Figure 1-2: MNOS FET

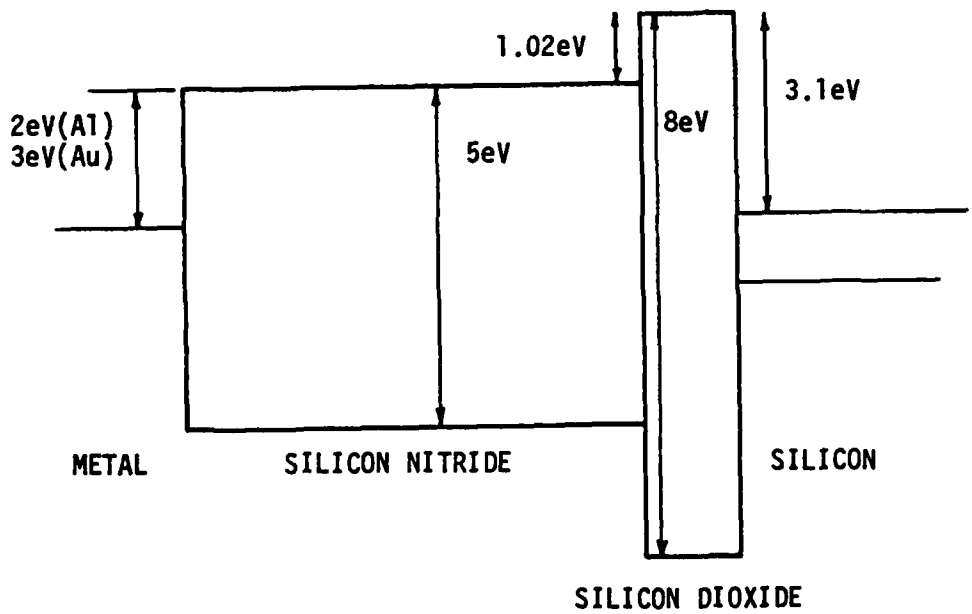


Figure 1-3: Ideal Energy Band Diagram for an MNOS Structure

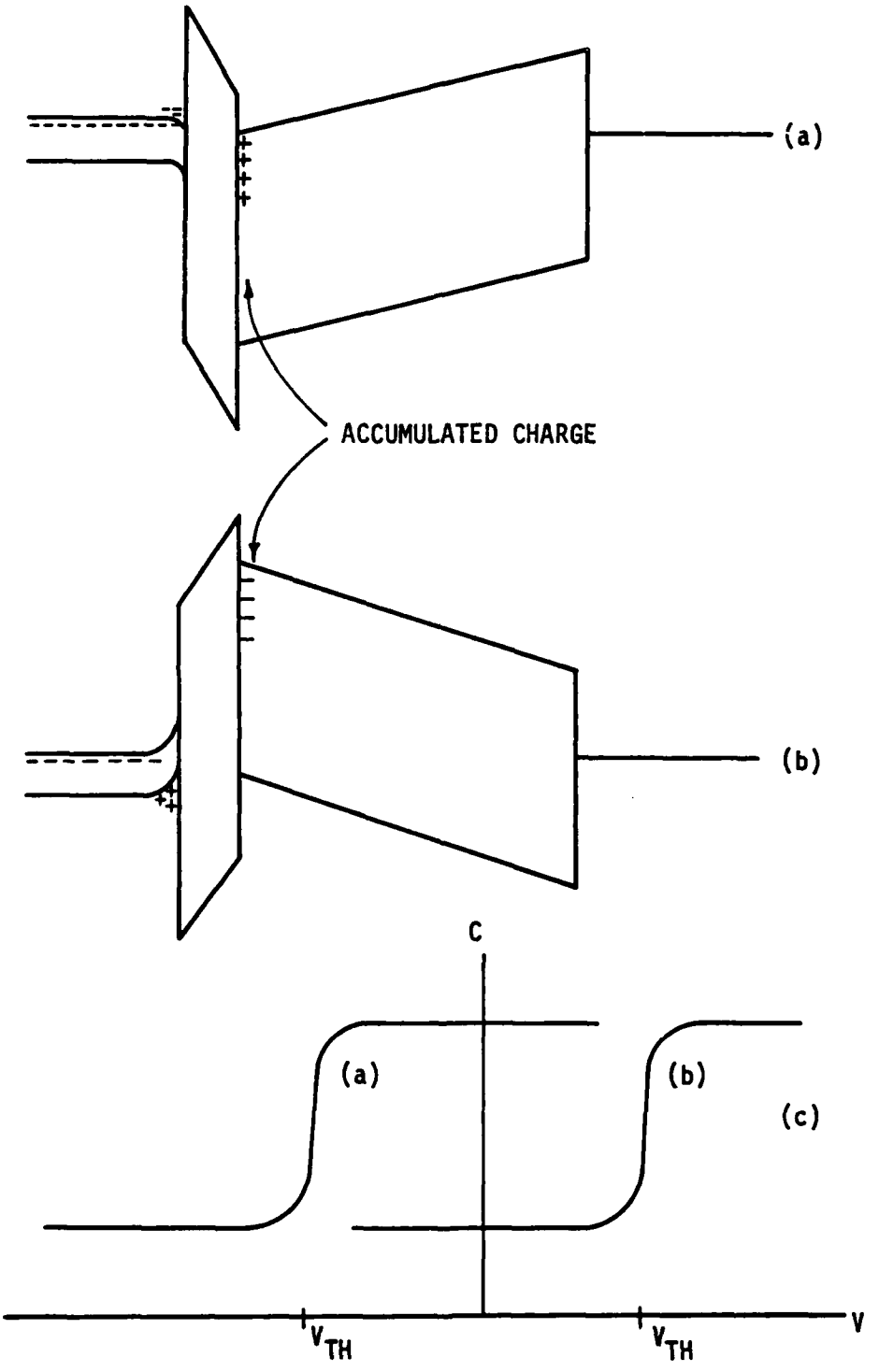


Figure 1-4: Typical Energy Band and C-V Diagrams for Positive and Negative Trapped Charge Conditions for an MNOS Structure

transistor can retain the high or low threshold voltage corresponding to its trapped charge condition for periods exceeding many years. By being able to accumulate and remove charges at the interface through application of large magnitude gate voltages of opposite polarity a two state memory device is obtained.

The initial devices studied had oxides more than 50 angstroms thick and nitrides up to 1000 angstroms thick [6, 8, 14]. These devices required greater than 30 volt bias pulses lasting up to a second to get appreciable threshold voltage shifts. Subsequent investigations have concentrated on MNOS structures with oxide layers less than 25 angstroms and nitride layers down to 200 angstroms thick, which allowed "write" or "erase" pulses on the order of 20 volts and down to 10 microsecond durations.

1.3 MNOS Charge Trapping

Many models and theories explaining charge trapping in the MNOS structure for various electric field regimes have been suggested [15]. Among them are (a) direct tunneling of electrons from the silicon conduction or valence bands, through the oxide, into traps in the nitride band gap; (b) Fowler-Nordheim emission of electrons from the silicon conduction band into the oxide conduction band, drift into the nitride conduction band and then trapping in nitride traps; (c) Modified Fowler-Nordheim emission of electrons from the silicon conduction band through the oxide and part of the nitride into the nitride conduction band and then charge trapping in nitride traps; (d) direct tunneling of electrons into nitride band gap traps near the oxide-nitride interface followed by detrapping into and retrapping from the nitride conduction

band; and (e) tunneling of holes from the silicon valence band into the nitride valence band and then trapping in the nitride.

1.3.1 Direct Tunneling

Direct tunneling to traps is generally accepted for charge transfer for thin oxide (<35 angstroms) devices under very low bias (low insulator electric field) conditions. Ross and Wallmark[16] proposed injection of electrons from the silicon valence band into monoenergetic traps in the center of the nitride band gap as shown in Figure 1-5. They indicated that at low bias conditions only the nitride traps furthest from the oxide-nitride interface would be opposite the valence band and available for filling by tunneling. At an increased bias, the traps closer to the oxide-nitride interface are able to communicate with the silicon valence band. The small tunneling probability at low bias conditions to traps deep in the nitride would effectively restrict trapping to within 35 angstroms of the oxide-nitride interface. Discharge was proposed to be accomplished under negative bias via electron tunneling from the traps to the silicon conduction band. Conduction in the nitride was ignored. Their expressions for threshold voltage shift are valid only for times greater than a defined transition time and do not show the observed threshold voltage shift saturation for large times. Goodman, Ross and Duffy[17, 18] presented experimental data which generally supported direct tunneling to monoenergetic traps, in the center of the nitride band gap, within 35 angstroms of the oxide-nitride interface. Dorda and Pulver[19] presented a theoretical approach which considered direct tunneling to traps uniformly distributed in energy at the oxide-nitride interface. They assumed that

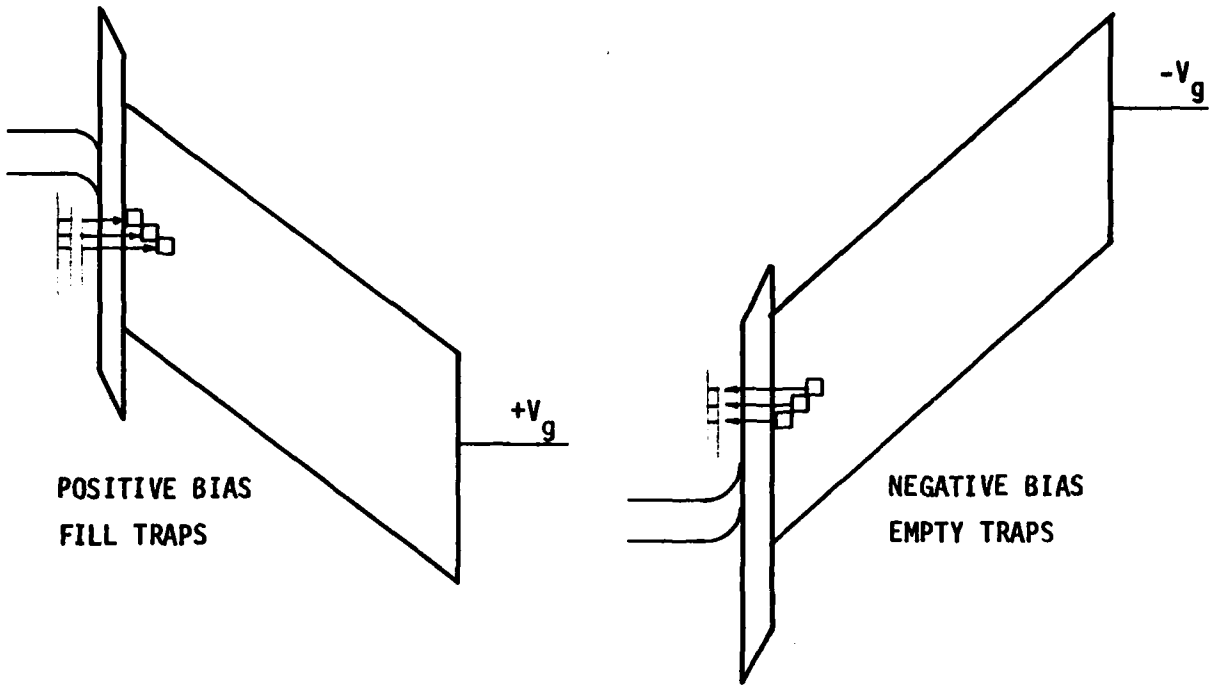


Figure 1-5: Direct Tunneling to Monoenergetic Traps in the Nitride of an MNOS Structure

all empty traps below the quasi-Fermi level participated in trapping under positive gate bias conditions and all filled traps higher in energy than the quasi-Fermi level participated in negative bias detrapping as shown in Figure 1-6. This development exhibits a zero and a saturated threshold voltage shift for applied bias times of zero and infinity respectively. White and Cricchi[20, 21] presented a development for direct tunneling to monoenergetic traps in the center of the nitride band gap and spatially located at the oxide nitride interface, but, additionally, introduced the concept of a finite nitride current to explain the threshold voltage shift saturation. They also described charge retention under zero bias as being controlled by back-tunneling from the oxide-nitride interface traps to the oxide-silicon interface states. Maes and Van Overstraeten[22] developed a low oxide field, theoretical expression for direct tunneling to traps in the nitride which were located approximately 1 eV below (above) the nitride conduction (valence) band. The 1 eV trap depth coincided with bulk nitride, Poole-Frenkel conduction, trap parameters referenced by Sze[23] and Frohman-Bentchkowsky[14]. Tunnel currents calculated using this expression agreed with an "excess" current measured by Lundstrom and Svensson[24] at low oxide fields. Ferris-Prabhu[25, 26, 27, 28] has considered nitride traps having both an energy and spatial distribution. His more exact analytical development is shown to reduce to the Ross and Wallmark treatment and the Dorda and Pulver expression under appropriate simplifying assumptions. To explain the lack of any threshold voltage shift for very long duration, low field conditions, he postulates a maximum tunneling distance in the nitride beyond which the trap density or charge trapping decreases rapidly. This distance is approximately 35

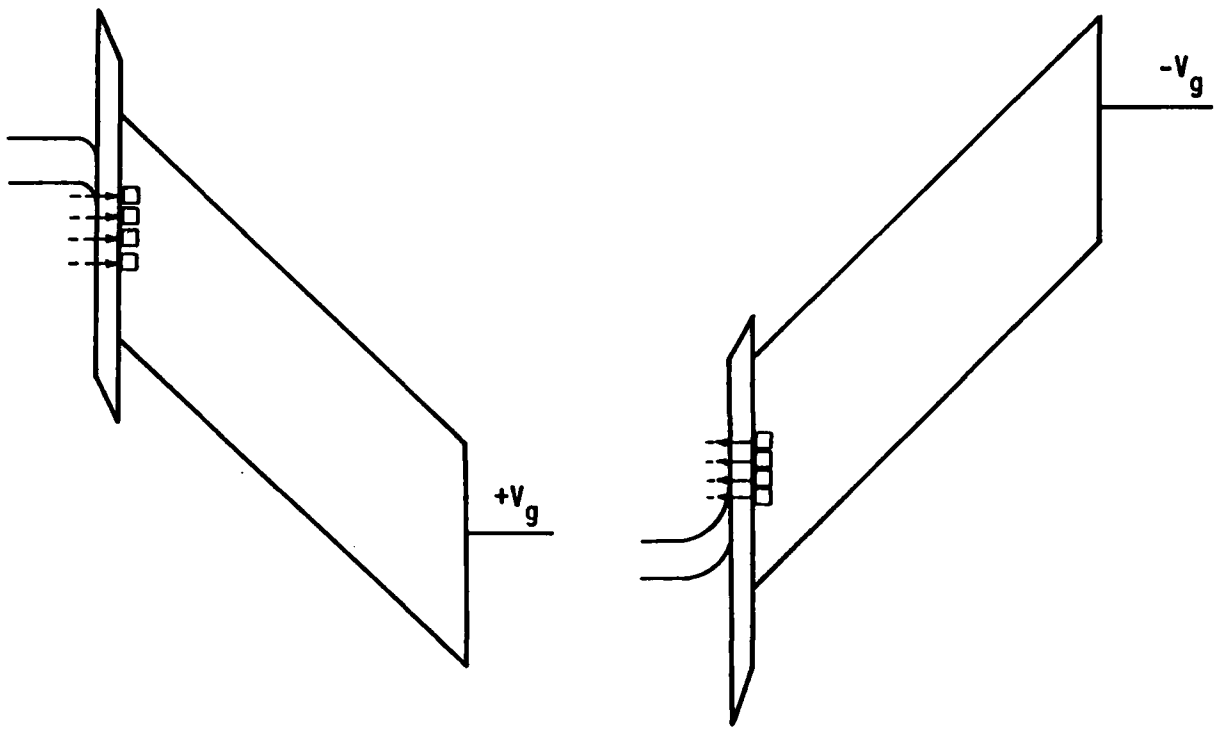


Figure 1-6: Direct Tunneling to Traps Uniformly Distributed in Energy in the Nitride of an MNOS Structure

angstroms. For very low fields, traps at this distance would be opposite the silicon band gap and no tunneling from conduction or valence bands would be possible. For very high fields no traps would be adjacent to the silicon forbidden band and therefore all traps could participate in tunneling action. Under this model there is no field dependence of charge trapping at very high fields. All the direct tunneling models assume only electron tunneling: from the silicon valence band into traps under positive gate bias and from traps into the silicon conduction band under negative gate bias.

1.3.2 Fowler-Nordheim Tunneling

Frohman-Bentchkowsky and Lenzlinger[14, 29] developed a model and analytical expressions for MNOS device operation for thick (>50 angstrom) oxide devices under high field conditions based on current continuity throughout the device. Fowler-Nordheim tunneling of electrons from the silicon conduction band into the oxide conduction band as shown in Figure 1-7 was assumed for the oxide current. The nitride current was expressed as a combination of ohmic conduction (low fields), Poole-Frenkel field enhanced thermal excitation (low temperature, high fields) and Schottky emission from traps (high temperature)[23]. The difference in the oxide and nitride currents would cause charge accumulation within 100 angstroms of the oxide-nitride interface.

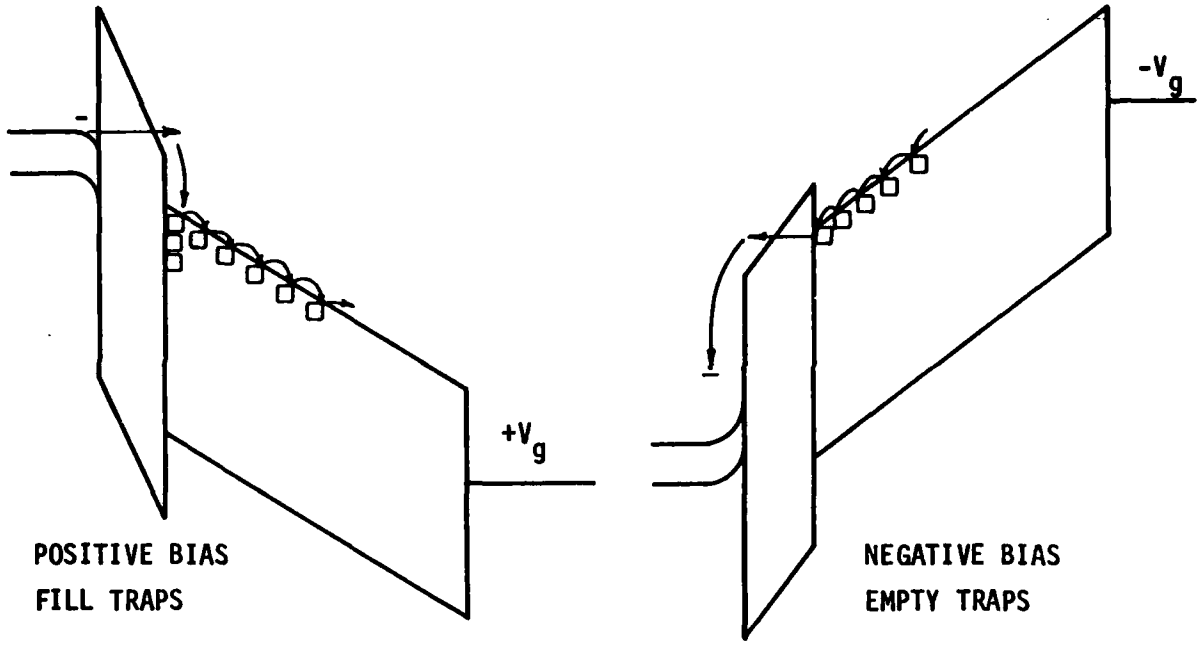


Figure 1-7: Fowler-Nordheim Emission into the Oxide Conduction Band in an MNOS Structure

1.3.3 Modified Fowler-Nordheim Tunneling

The Fowler-Nordheim charge injection model was extended to thin oxide (<50 angstrom) devices by Svensson and Lundstrom [24, 30, 31] by proposing a modified Fowler-Nordheim electron current which penetrates the total oxide thickness and part of the nitride. Under positive gate bias, electrons are injected from the silicon conduction band into the nitride conduction band. Trapping in bulk nitride follows. This is shown in Figure 1-8. The trapped charge is removed under negative gate bias via two phenomena: (1) direct tunneling of electrons from the nitride traps through the nitride and oxide into the silicon conduction band and (2) tunneling of holes from the silicon valence band into the nitride valence band, followed by hole trapping and trapped electron-injected hole recombination. This model implies trapping in the bulk of the nitride, away from the oxide-nitride interface. Calculations, however, were based on the assumption of charge accumulation only at the oxide-nitride interface. Gordon and Johnson [32] present pulse and dc data which qualitatively support the modified Fowler-Nordheim model. The trap depth and distribution in the nitride were not addressed in either investigation. Svensson and Lundstrom considered a nitride current, but that was introduced only in the calculation of the maximum stored charge (threshold voltage shift at saturation). Beguwala and Gunchel [33] combined the low field, modified Fowler-Nordheim injection, high field Fowler-Nordheim tunneling and Poole-Frenkel nitride conduction for all applied bias to compute a full range of write/erase characteristics. These calculations, although developed under the assumption of charge trapping only at the oxide-nitride interface, attempted to consider the effect of charge

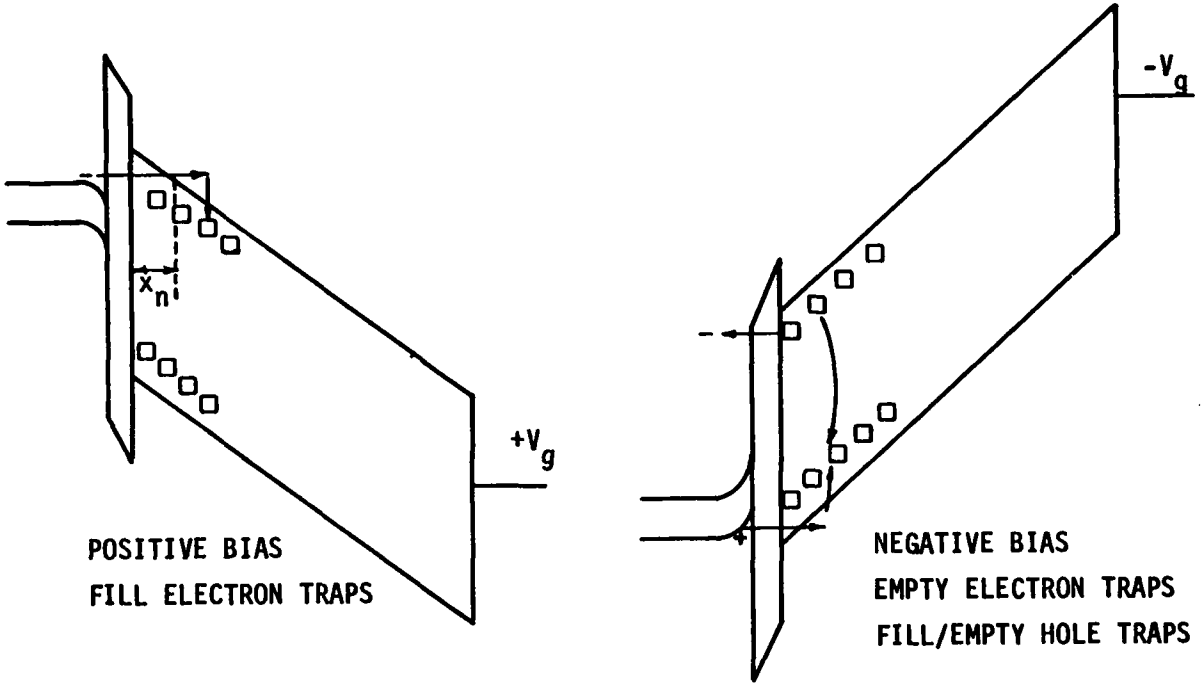


Figure 1-8: Modified Fowler-Nordheim Tunneling into the Nitride Conduction or Valence Band in an MNOS Structure

distribution in the nitride. This was accomplished by introducing a curve fitting constant which was described as being a function of charge centroid and nitride thickness ratio. A value of approximately 0.5 for this ratio was used. These developments departed from the direct tunneling model by assuming electron injection from the conduction band and hole injection from the valence band.

1.3.4 Trap Assisted Charge Injection

Svensson and Lundstrom[34] proposed a low field charging mode that combined their modified Fowler-Nordheim injection model with that of direct tunneling to traps. Under positive gate bias, electrons would tunnel through the oxide and part of the nitride into traps approximately 0.7 eV below the nitride conduction band in the bulk nitride. Only traps which were lowered by the applied bias to be approximately at the silicon conducton band energy would participate. Higher gate bias would permit traps closer to the oxide-nitride interface to assist in the charge injection process. Figure 1-9 shows this. These traps then empty into the nitride conduction band with a time constant shorter than the tunneling time constant. Nitride conduction band electrons would then be retrapped in permanent trapping locations. Discharge under negative bias would involve hole tunneling from the silicon valence band into nitride traps approximately 1 eV above the nitride valence band. These trapped holes then must recombine with the trapped electrons. Maes and Van Overstraeten[35] used a combination of transient and dc data to support the trap-assisted tunneling mechanism for low fields and Fowler-Nordheim tunneling at high fields. Both investigations ignored conduction in the nitride,

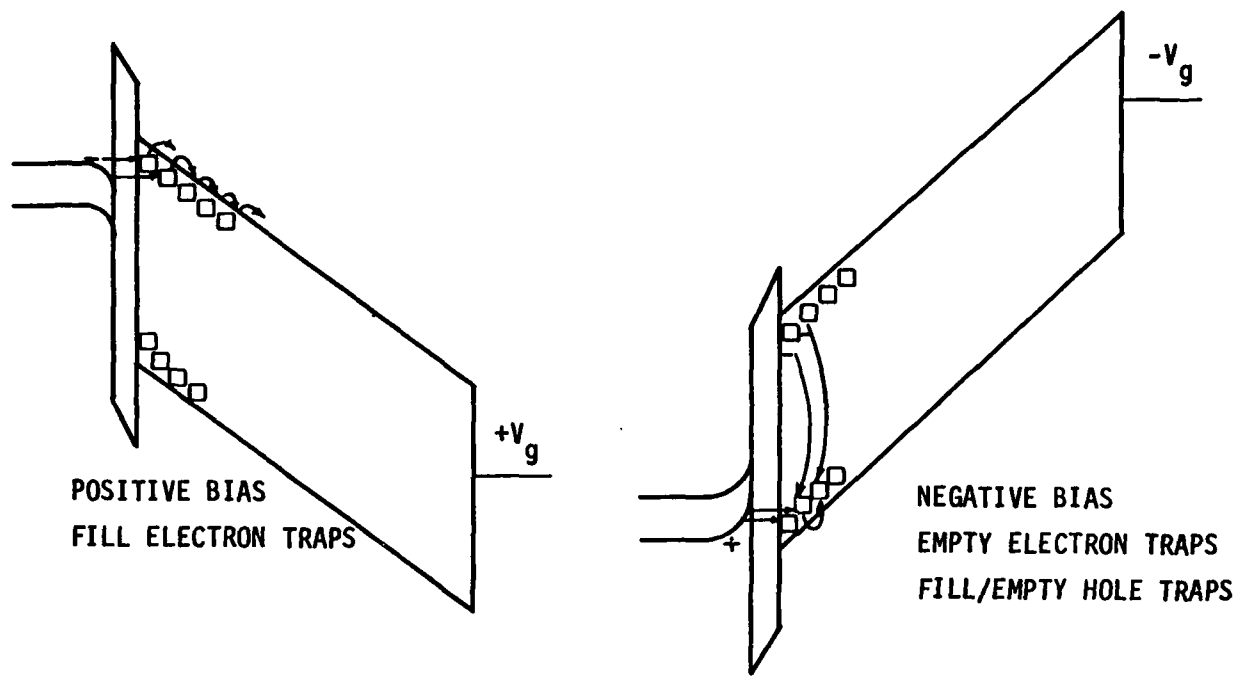


Figure 1-9: Trap Assisted Tunneling through the Oxide into the Nitride of an MNOS Structure

described tunneling to, and emission from, traps located at distances greater than 50 angstroms from the oxide while assuming all charges were accumulated at the oxide-nitride interface, and did not discuss the permanent memory traps versus the tunneling assisting traps.

1.3.5 Hole Tunneling

No one has proposed a charge trapping and detrapping sequence based entirely on hole motion. The proponents of Fowler-Nordheim injection, modified Fowler-Nordheim tunneling and trap assisted tunneling techniques propose hole tunneling as one phenomenon operating under negative gate bias conditions. Experiments have been performed to attempt to determine absolutely which carriers play the dominant roles in MNOS device operation. Noting that the MNS fabrication process which requires that a freshly etched silicon substrate be transported to the nitride deposition facility and then heated to a nitride deposition temperature normally greater than 750°C unavoidably leads to some silicon oxide growth prior to nitride deposition, devices fabricated as MNS structures would tend to have an unintentional MNOS structure. Yun[36] and Mickanin and Gordon[37] have made measurements using intentionally fabricated MNOS structures and Weinberg and Pollak,[38] Arnett and DiMaria,[39] Svensson,[40] and Arnett and Weinberg[41] fabricated metal-nitride-semiconductor (MNS) structures for their measurements. All the reported results do indicate definite hole injection from the silicon under negative gate bias. However, the results under positive gate bias are inconclusive regarding the dominance of hole injection from the metal into the nitride or from the nitride into the silicon valence band as compared to electron injection.

1.4 Retention(Zero Bias Discharge)

In addition to charge trapping and detrapping under large magnitude bias voltages, the phenomenon of retention of charge, or zero or low bias discharge, has been considered. Lundkvist et al[42, 43] developed an explaination of discharge based on direct tunneling of trapped electrons (holes) from nitride gap traps near the nitride conduction (valence) band edge into the silicon conduction (valence) band and thermal excitation of electrons (holes) out of nitride traps into the nitride conduction (valence) band. These charge movements are shown in Figure 1-10. Their discussions did not address the movement of the charges after Excitation out of traps. A figure in reference [43] appears to imply charge drift toward the oxide-nitride interface, presumably followed by tunneling into the silicon. Following definite evidence of trapped charge penetration considerable distances into the nitride,[44, 45] the redistribution of charges deeper into the bulk of the nitride was included as an addition to the technique of direct back-tunneling of charges into the silicon in proposed zero bias discharge models.[10, 11, 46, 12]

1.5 Endurance

One other characteristic of the MNOS system that has been a point of discussion is endurance, or the ability of the MNOS device to undergo write/erase cycling and still be able to exhibit a usable two-state memory characteristic. The degradation of MNOS performance after limited high voltage operation was observed by Cricchi and Read.[47] Woods and Tuska[48] and Cricchi et al[49, 50] observed the reduction in the memory "window" (difference between FET threshold voltage values for similar

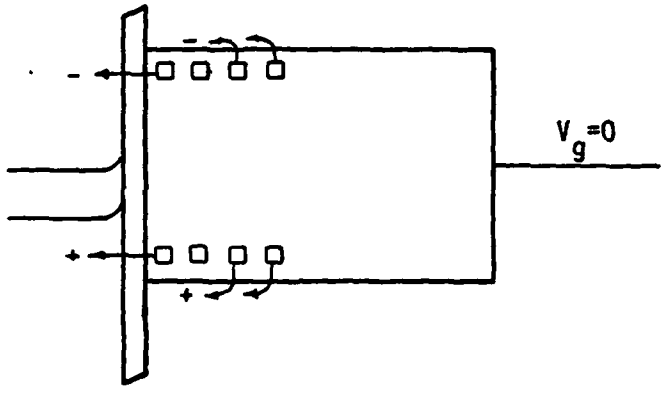


Figure 1-10: Discharge via Direct Tunneling and Thermal Excitation in an MNOS Structure (From [43])

positive and negative, write/erase, pulses) and a negative shift in the voltage at the center or mid-point of the window following write/erase cycling and attributed these effects to formation of fast surface states at the silicon-silicon dioxide interface and in the thin oxide itself. Schuermeyer et al[51] performed charge pumping experiments to show surface state creation during write/erase cycling. Additional experimental verification of the fast surface state generation was presented by Jeppson and Svensson[52, 53] and Schauer et al.[54] By studying MOS and MNOS structures Jeppson proposed generation of hole traps in the oxide as additional contributors to endurance degradation. Following the definite evidence of charge penetration into the bulk of the nitride,[10, 45, 55] White et al[56, 57] and Neugebauer and Burgess[58] presented developments which indicated that part of the endurance problem stemmed from some charge being permanently trapped deep in the nitride. Gentil and Chausse[59] also present data which support the generation of hole traps in the oxide.

Endurance is intimately related to retention. When endurance is expressed in terms of write/erase cycles and retention in terms of seconds commercial devices exhibit a retention-endurance product less than 5×10^{14} cycle seconds. Laboratory MNOS devices have shown retention-endurance products up to 10^{16} cycle seconds.[60] This implies a 3×10^{7} cycle maximum endurance for a 10 year retention requirement.

1.6 Interface Doped Dual Dielectric Cell

MNOS electrically alterable, non-volatile, memories are commercially available today. However, they are "read mostly" devices (memory degradation occurs in less than 10^7 write/erase cycles even for a retention period of one year duration) which generally require greater than twenty volt, one millisecond, write pulses and longer erase pulses. The reasons for the restriction to "read mostly" and the undesirably high magnitude, long duration pulse parameters include: (1) a high magnitude, long pulse is required to inject charges and create a threshold voltage shift (the threshold window) needed to produce the two definite memory states; (2) the fatigue or lack of endurance, as described in Section 1.5. This latter effect is presently attributed to charges becoming permanently trapped in deep traps in the nitride bulk, far from the oxide-nitride interface, and which therefore, cannot communicate readily with the silicon and to the creation of silicon-silicon dioxide surface states which enhance back tunnelling of electrons from the oxide-nitride interface, through the oxide into the silicon. The existance of trapped charges deep in the nitride in MNOS devices has been shown.[44, 45, 61] The result of fatigue is that after many write/erase cycles (the "endurance" of the device), the threshold voltage cannot be made to shift sufficiently, hence the threshold window becomes too small to allow unambiguous determination of the state of the memory device. A sufficiently large shift of the window center voltage can cause an existing threshold voltage window to shift such that the "read" voltage applied to the gate to determine the state of the memory device will produce the same readout whether the device is in a written or erased condition.

A recent improvement suggested for MNOS devices involves "doping" the oxide-nitride interface.[1] Doped MNOS devices have improved writing and retention characteristics (smaller and shorter write/erase pulses producing similar threshold voltage windows and retention times)[62] and an improved endurance was initially predicted. It was suggested that the improvements were due to an increased trap density at the oxide-nitride interface which would then prevent charge trapping deep in the bulk of the nitride. This development was an extension of earlier attempts to create and improve non-volatile semiconductor memory devices.[63] Kahng and Sze proposed a device composed of a metal or semiconductor substrate, a thin insulator, a metal film, a thick insulator and a metal top contact. They fabricated a MIMIM (or SIMIM) in the form of a silicon-silicon dioxide(50 angstroms)- zirconium(1000 angstroms)-zirconium oxide(1000 angstroms)-metal structure. Memory retention was on the order of an hour.[64] Laibowitz and Stiles modified the structure by proposing an ultra thin metal film between the dielectrics, effectively creating a layer of small metal particles due to the agglomeration of thin deposited metal films. Their silicon-silicon dioxide(25 angstroms)-platinum(35 angstroms)- aluminum oxide(750 angstroms)-metal structure exhibited a 10 volt threshold voltage shift for 15 volt write/erase bias conditions and no charge loss over periods of several hours.

The doping proposed by Kahng[1] consists of an electron beam evaporated deposit of metal, on the order of 10^{15} atoms/cm^2 (less than a monolayer), at the oxide-nitride interface. This procedure produces devices which, when compared to conventional, undoped, devices, exhibit

the same threshold voltage shift when using lower amplitude write/erase pulses, exhibit the same threshold voltage shift when using shorter write/erase pulses, and have retention times as great or greater than conventional devices. The pulse parameter improvement is attributed to the dopant creating traps such that most of the device charge is trapped at the interface of the dielectrics, not in the thick insulator (silicon nitride or aluminum oxide) bulk. The retention improvement is considered to be the result of being able to use thicker oxide layers (>50 angstroms) and still have moderate voltage write/erase operation because of the localized charge trapping. Neugebauer[2, 3, 65] has measured similar write/erase and retention improvements but has also reported reduced endurance for interface doped devices, contrary to the increased endurance expected by the hypothesis that localized charge trapping would prevent permanent, deep trap, trapping in the nitride bulk since this bulk nitride trapping is presently thought to be the prime cause of lack of endurance in MNOS devices. His work did not develop information which would explain why the measured endurance is so reduced for interface doped devices.

The operational parameters of doped dual dielectric cells and various techniques for fabricating the devices have been studied. Vitanov et al[66] formed the dopant deposition by evaporating a 2000 angstrom thick film of tungsten and then etching it "completely" off. DC bias write/erase and retention characteristics showed the improvement over non-doped devices. Yoshino et al[67, 68] formed silicon dioxide(27 angstroms)-platinum(10 angstroms)-silicon dioxide dual dielectric structures and subjected them to various post fabrication heat

treatments and auger analysis. As fabricated, the devices showed excellent write/erase characteristics, poor retention and a platinum distribution which penetrated the thin oxide. After an extended heat treatment in an oxygen atmosphere the write/erase characteristics degraded, the retention was excellent and the platinum distribution was separated from the silicon surface by over 100 angstroms of oxide. The oxygen had penetrated through to the silicon surface and formed additional silicon oxide beneath the deposited platinum. The "augmented" oxide was sufficiently thick that it reduced the write/erase tunnel currents and reduced the zero bias discharge. Ligenza et al[69] recognized that, in the process of tungsten dopant deposition on the thin oxide layer followed by thick insulator growth, the tungsten has a high likelihood of being oxidized. They have used low temperature tungsten trioxide evaporation as a convenient, production oriented, method to produce devices as efficient as those made using very high temperature tungsten evaporation for dopant deposition. Neugebauer and Barnicle[2, 3, 65] accomplished an in-depth experimental study of the effects of varying oxide thickness, dopant species, dopant density and dopant deposition technique on MNOS device operational characteristics for both p-channel and n-channel FET use.

1.7 Research Approach

1.7.1 Fabrication

The initial portion of this research involved developing a process for device fabrication, particularly the thin oxide production, dopant deposition and nitride deposition. Techniques were developed to controllably grow 30 to 100 angstrom oxides, deposit the tungsten dopant

over the range of 7×10^{14} to 7×10^{15} atoms per square centimeter and deposit silicon nitride on five wafers at a time with an across-the-wafer and a wafer-to-wafer thickness variation of less than fifteen angstroms for a nominally 400 angstrom nitride layer. Capacitors having MOS, MNS, MNOS and interface doped MNOS (DMNOS) structures were fabricated.

1.7.2 Measurements

This investigation assumed an MNOS device model having silicon-silicon dioxide interface states with a continuous energy distribution, a trap-free oxide, oxide-nitride interface states with one or more distinct energy levels or bands, dopant induced traps at the oxide-nitride interface with one or more distinct energy levels or bands, and bulk nitride traps having distinct energy levels. Injected charge spatial densities were examined through the use of total trapped charge and charge centroid measurements on MNOS[10] structures. Trap energy densities were examined using thermal excitation of trapped charges (thermally stimulated current (TSC) measurements).

TSC experiments on MNS capacitor structures yielded the bulk nitride trap levels and silicon-silicon nitride interface states. The oxide-nitride interface states and bulk nitride traps active for MNOS devices were investigated using conventional MNOS device structures. Investigation of doped MNOS devices assumed the continued validity of the trap data obtained on MNS and conventional MNOS structures. Additional trap levels evident in DMNOS measured TSC data were attributed to the dopant at the oxide-nitride interface and absence of trap levels found in MNS structures was attributed to the

silicon-silicon nitride interface. These investigations provide the first measurments of the energy levels of the dopant-induced traps.

1.7.3 Model

From an analysis of the above data, a model of the trapping levels in DMNOS structures was formed. This model, augmented by theoretical expressions for charge conduction in the oxide and nitride and appropriate assumptions for charge and discharge mechanisms, was used to calculate write/erase and charge centroid characteristics for comparison to measured data from this study and that published by others.

1.8 Summary of Results

1.8.1 Charge Centroid

Data relating charge centroid as a function of injected charge was obtained for a standard MNOS structure with a 32 angstrom oxide, for interface doped MNOS structures with 32 angstrom oxides and having light doping ($<10^{15}$ tungsten atoms per square centimeter) and heavy doping ($>2 \times 10^{15}$ tungsten atoms per square centimeter) and for an interface doped MNOS structure with a 52 angstrom oxide and light doping. The standard device exhibited a consistent 200 ± 50 angstrom centroid at charge injection levels from less than 10^{11} to greater than 10^{13} electrons per square centimeter. The doped devices demonstrated charge trapping at the oxide-nitride interface (charge centriod equal to 0 ± 25 angstroms) at charge injection levels from 4×10^{11} charges per square centimeter up to a trap "saturation" value which depended on the oxide thickness rather than dopant density. For charge injection above the "saturation" level, the charge centroid gradually penetrated into the

bulk nitride as deep as for the standard MNOS devices. The saturation level for the 32 angstron oxide DMNOS devices was 6 x 10^{12} charges/cm^2 while for the 52 angstrom oxide device the saturation level was 1 x 10^{12} charges/cm^2.

1.8.2 Charge Trapping Levels

Thermally stimulated charge emission measurements were made on MNS, MNOS (35 and 80 angstrom oxides) and DMNOS (35 and 80 angstrom oxides, 7 x 10^{14} and 7 x 10^{15} tungsten atoms cm^{-2} dopant) devices. Trap depths below the silicon nitride conduction band energy level were calculated for the bulk nitride, the oxide-nitride interface and the interface dopant and below the silcon conduction band for the silicon-silicon dioxide interface. These are tabulated in Table 1-1.

Trap Location	Trap Depth (eV)	Maximum Trap Density (cm^{-2})	(cm^{-3})
Nitride	1.14 - 1.19	5 x 10^{12}	1.5 x 10^{18}
	1.35 - 1.38	5	1.2
	1.40 - 1.43	4	1.1
	1.47 - 1.58	4	1.0
	1.92 - 2.04	32	8.0
	2.05 - 2.14	12	3.0
	2.15 - 2.32	12	4.0
Oxide-nitride	0.70 - 0.93	6	
	1.30 - 1.34	30	
Interface Dopant	1.71 - 1.79	4	
	1.82 - 1.86	6	
Silicon-silicon dioxide	0.3 - 0.5	0.1 (Virgin) 5 (High Field Stressed)	

Table 1-1: Trap Energy Levels and Spatial Densities

1.8.3 Trap Density

Trapped charge emission from the various trap levels were used to deduce the maximum trap densities shown in Table 1-1.

1.8.4 Model Verification

These parameters were then used to form the trap configuration shown in Figure 1-11.

To complete the model of charge trapping in the interface doped device the following assumptions were made:

Charge Injection Assumptions (Figure 1-12 shows charge motion):

- Electrons are injected from the silicon conduction band, through the oxide, into the nitride conduction band. A Fowler-Nordheim type injection equation is used to express the oxide electron current.
- A portion of the electrons are trapped at the oxide-nitride interface. Trapping is proportional to capture cross section, and number of empty traps.
- Electrons are detrapped from the oxide-nitride interface via Poole-Frenkel type field assisted thermal emission into the nitride conduction band.
- Injected electrons in the nitride conduction band undergo a trapping/detrapping process through the nitride layer, determined by the nitride traps parameters, trap occupancy, temperature and electric field.

Discharge Assumptions (Figure 1-13 shows charge motion):

- Holes are injected from the silicon valence band, through the oxide, into the oxide valence band. A Fowler-Nordheim type injection equation is used to express the oxide hole current.
- A portion of the holes are trapped at the oxide-nitride interface at trapped electron sites. Trapping is proportional

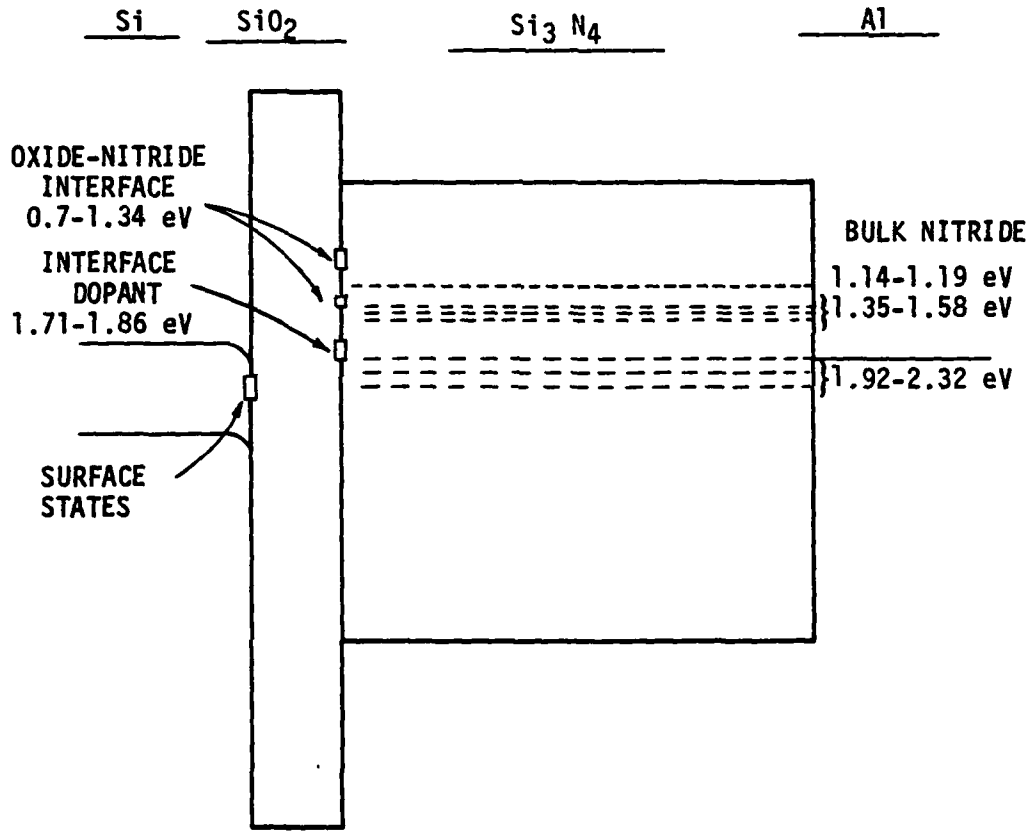


Figure 1-11: Trap Configuration-Interface Doped MNOS

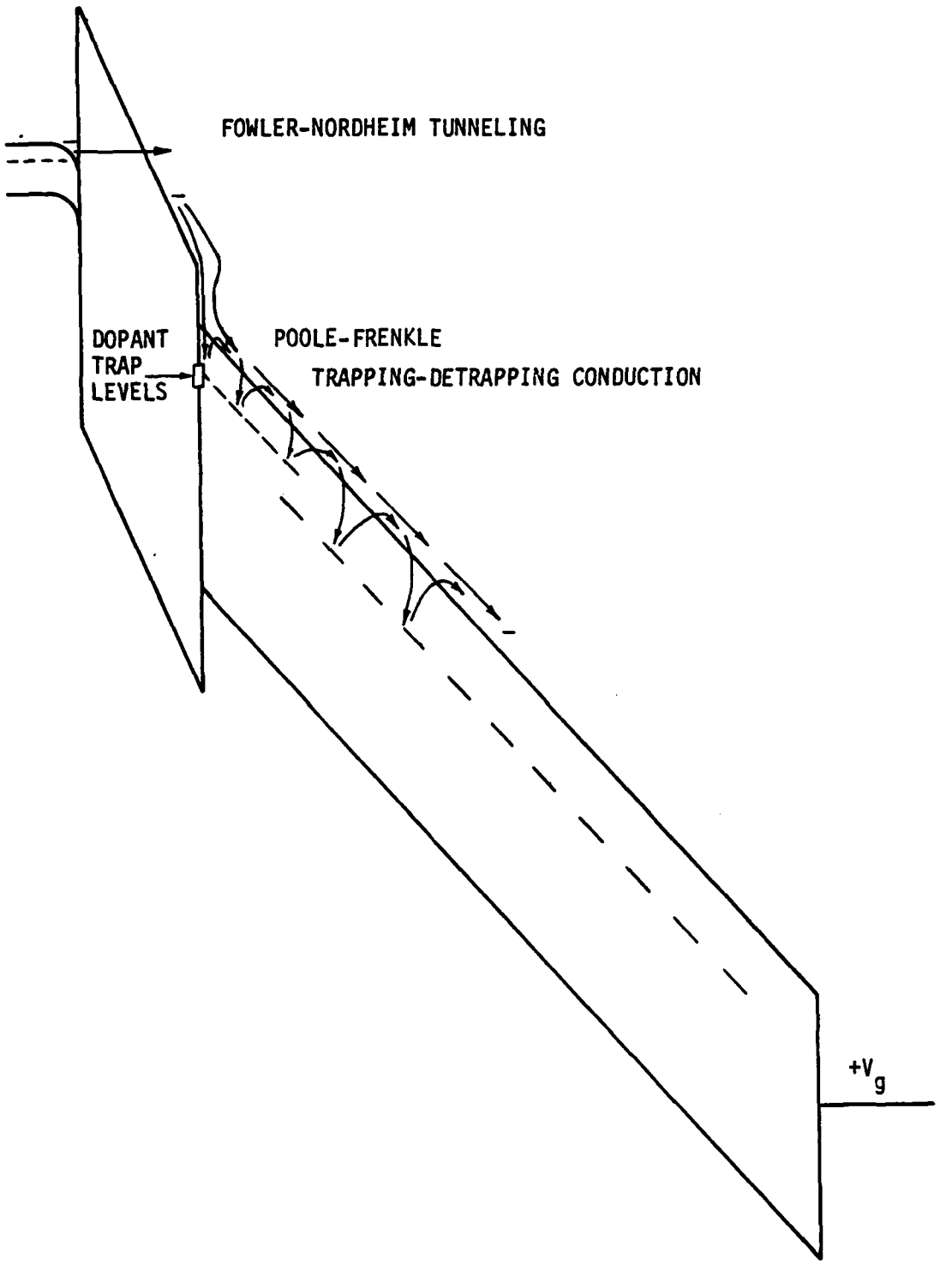


Figure 1-12: Charge Injection Process under Positive Bias into an MNOS Structure

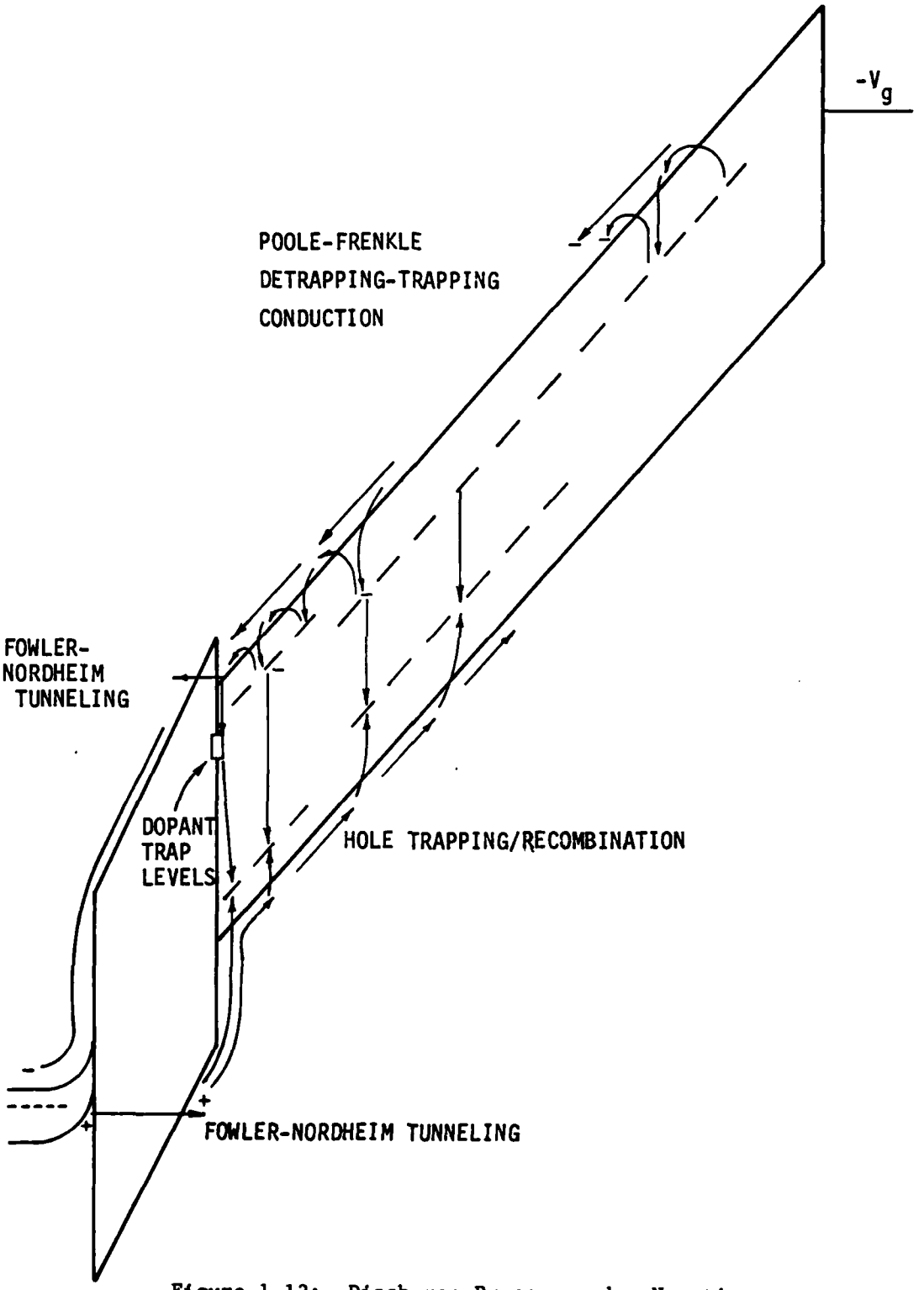


Figure 1-13: Discharge Process under Negative Bias for an MNOS Structure

to capture cross section and number of trapped electrons.

- Trapped holes recombine with trapped electrons immediately. There is no hole detrapping.

- Injected, non-trapped, holes remaining in the nitride valence band undergo trapping and recombination with trapped electrons while traversing the nitride toward the gate.

- Simultaneously, electrons undergo a detrapping and retrapping process, traversing the nitride toward the oxide-nitride interface.

- At the oxide-nitride interface, electrons detrapped from the interface and any nitride conduction band electrons (the portion of electrons detrapped at the oxide-nitride interface or from the bulk nitride but not retrapped while traversing the bulk) participate in a Fowler-Nordhein type tunneling through the oxide into the silicon conduction band.

Calculated Results

From these assumptions calculations were made of the charge distribution, the centroid vs injected charge and flatband (threshold) voltage shift vs gate voltage pulse width (write/erase characteristics) for interface doped and standard MNOS devices. The predicted write/erase and centroid characteristics agree well with measured data. Additionally, this proposed model provides a qualitative explaination of observations made by Neugebauer[65] based on his measurements on conventional and interface doped MNOS structures.

1.9 Chapters 2 - 5

The following chapters will present the experimental approach, the theoretical basis of data analysis and measured and calculated results of the charge centroid measurements (Chapter Two) which resulted in injected charge, centroid vs time and centroid vs injected charge data,

and the thermally stimulated current measurements (Chapter Three) which resulted in emitted charge, current (emitted charge) vs temperature, trap energy levels and trap densities for MNS, MNOS and DMNOS structures. Chapter Four describes the MNOS model, the basis of parameters used in the tunneling, trapping and detrapping expressions and presents a comparison of device characteristics determined by the model as compared to measured data taken during this investigation and other published data. Chapter Five presents conclusions of this study, limitations of the model and recommendations for additional efforts.

2. CHAPTER TWO - CHARGE CENTROID

2.1 Theory

Initial efforts in the study of the MNOS structure as a memory device assumed all the trapped charges were located at the oxide-nitride interface or just inside the nitride (less than 50 angstroms from the interface).[15] However, the appearence of fatigue, or voltage threshold window closure, in MNOS devices suggested that there could be appreciable charge trapping within the bulk nitride. Two techniques were developed to examine the distribution of charge within the bulk nitride.[44, 10, 45, 61] These new techniques were required because conventional measurements on metal-insulator-semiconductor(MIS) devices only yield the product of total trapped charge and the distance to the charge distribution center (charge-charge centroid product). Before describing the charge centroid measurement techniques, a comparison between the well known MOS flatband voltage-charge relationship and that for the MNOS structure will be developed.

2.1.1 MOS/MNOS Flatband Voltage-Charge Relations

MOS Expressions

The development in this section follows that of standard references on this subject.[70, 71, 72] General band diagrams for an MOS structure under zero and inversion creating negative bias conditions are shown in Figure 2-1 for an n-type substrate material. The charge distribution in each case is shown in Figure 2-2.

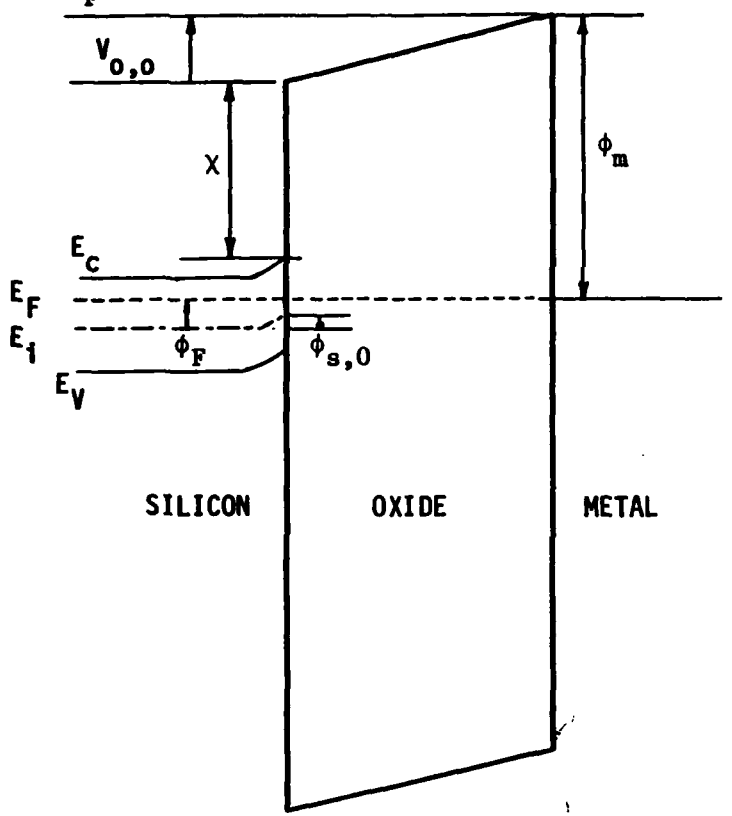
V_o and $V_{o,0}$ = Voltage across oxide

ϕ_s and $\phi_{s,0}$ = Semiconductor surface potential

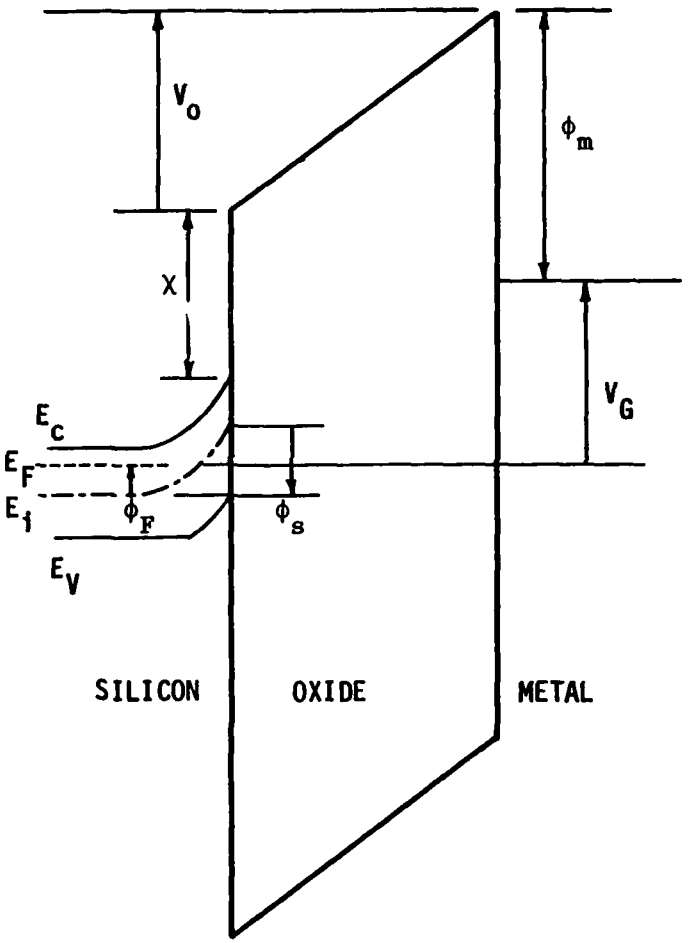
χ = Semiconductor electron affinity

ϕ_m = Metal work function

ϕ_F = Fermi potential



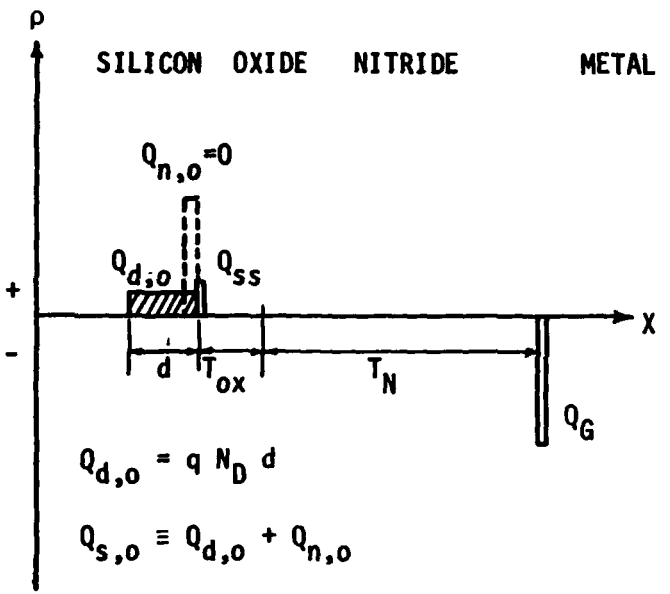
Zero Bias



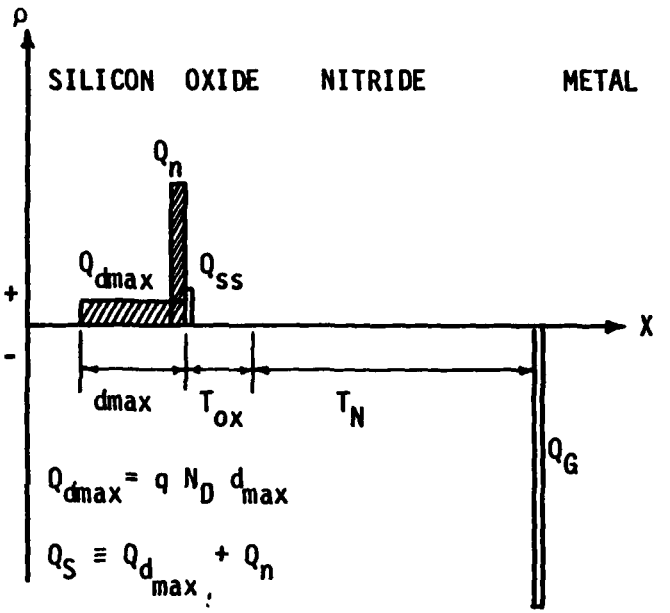
Negative Bias on Metal Gate
(Inversion Condition)

Figure 2-1: MOS Band Diagrams

Zero Bias



Negative Bias on Metal Gate
(Inversion Condition)



Q_G = Charge on the metal gate

Q_{ss} = Fixed semiconductor surface charge

Q_n and $Q_{n,0}$ = *Inversion layer charge*

Q_d and $Q_{d,0}$ = Depletion layer charge

Q_s and $Q_{s,0}$ = Total charge inside semiconductor

Figure 2-2: MOS Charge Distribution

The metal-semiconductor work function difference is defined as:

$$\phi_{ms} \equiv \phi_m - (\chi + \frac{1}{2}E_g + \phi_F) \tag{2.1}$$

From Figures 2-1 and 2-2 and equation (2.1):

$$V_G = V_o + \phi_s + \phi_{ms}$$

$$Q_G + Q_{ss} + Q_d + Q_n = 0$$

Therefore:

$$V_G = (-Q_{ss} - Q_d - Q_n)T_{ox}/\varepsilon_{ox} + \phi_{ms} + \phi_s$$

$$= -(Q_{ss} + Q_d + Q_n)/C_o + \phi_{ms} + \phi_s$$

where: T_{ox} is the oxide thickness

$C_o = \varepsilon_{ox}/T_{ox}$ is the oxide capacitance per unit area

Two parameters referred to in discussing MOS or MNOS devices are flatband voltage and threshold voltage. Flatband voltage is the gate voltage required to cause the energy bands in the semiconductor to flatten out. Under this condition $\phi_s = 0$ and $Q_n = Q_d = 0$. Therefore:

$$V_{FB} = -Q_{ss}/C_o + \phi_{ms} \tag{2.2}$$

The threshold voltage for an FET is the gate voltage at which the surface has become just inverted and for which a detectable drain current will flow for a specific drain voltage. Analytically it is defined as the voltage for "strong inversion", that is the minority carrier concentration at the surface equals the bulk inpurity concentration. This will be achieved for $\phi_s = 2\phi_F$. Additionally, the simplifying assumptions of $Q_n = 0$ and Q_d equal to its maximum value Q_{dmax} (any increase in Q_s due to additional gate bias will only affect Q_n) are usually made. Under these conditions:

$$V_{TH} = (-Q_{ss} - Q_{dmax})/C_o + \phi_{ms} + 2\phi_F \qquad (2.3)$$

The next step in complexity is considering fixed charges in the oxide as shown in Figure 2-3. For no applied bias (and ideal case of $\phi_{ms} = 0$) the electric field-charge relationships are:

$$F_2 - F_1 = Q_{ox}/\varepsilon_{ox}$$

$$F_1 x + F_2(T_{ox} - x) = 0$$

$$Q_s = \varepsilon_{ox} F_1$$

Therefore the charge induced in the semiconductor by the fixed oxide charge Q_{ox} is:

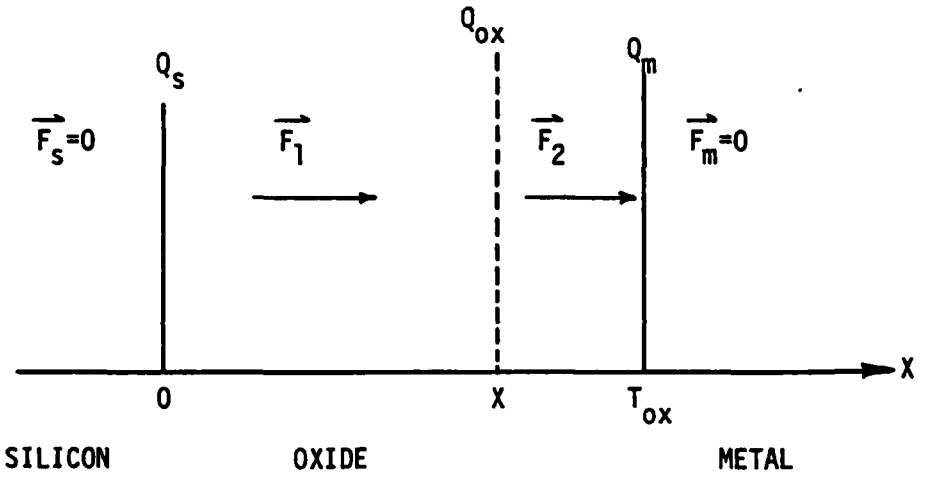


Figure 2-3: MOS With Fixed Oxide Charges

$$Q_s = -Q_{ox}(1 - x/T_{ox})$$

This Q_s could be considered as being produced by an "effective" surface charge at x = 0,

$$Q_{eff} = -Q_s = Q_{ox}(1 - x/T_{ox})$$

This Q_{eff} then can be added to the naturally occuring Q_{ss} which was included in expressions (2.2) and (2.3) developed for flatband and threshold voltage, ie:

$$V_{FB} = \phi_{ms} - (Q_{ss} + Q_{eff})/C_o \tag{2.4}$$

and

$$V_{TH} = \phi_{ms} + 2\phi_F - (Q_{ss} + Q_{eff} + Q_{dmax})/C_o \tag{2.5}$$

If a charge distribution in the oxide is considered, a differential element dQ_{eff} can be defined from which the total Q_{eff} is described by:

$$dQ_{eff} = \rho(x)dx\ (1 - x/T_{ox})$$

$$Q_{eff} = \int_o^{T_{ox}} \rho(x)(1 - x/T_{ox})dx$$

This then can be a part of Q_{eff} in equation (2.4) and (2.5).

MNOS Expressions

In the MNOS structure the principles are the same, except that a few more parameters are added. For no charge at the oxide-nitride interface the band diagrams are as shown in Figure 2-4 and charge distributions in Figure 2-5. Again, from charge neutrality and sum of potentials considerations:

$$V_G = V_N + V_o + \phi_{ms} + \phi_s$$

where ϕ_{ms} is as defined in Equation (2.1)

$$Q_G + Q_{ss} + Q_n + Q_d = 0$$

hence

$$V_G = -(\varepsilon_{ox})^{-1} (Q_{ss} + Q_n + Q_d) (T_{ox} + T_N \varepsilon_{ox}/\varepsilon_N) + \phi_{ms} + \phi_s$$

or

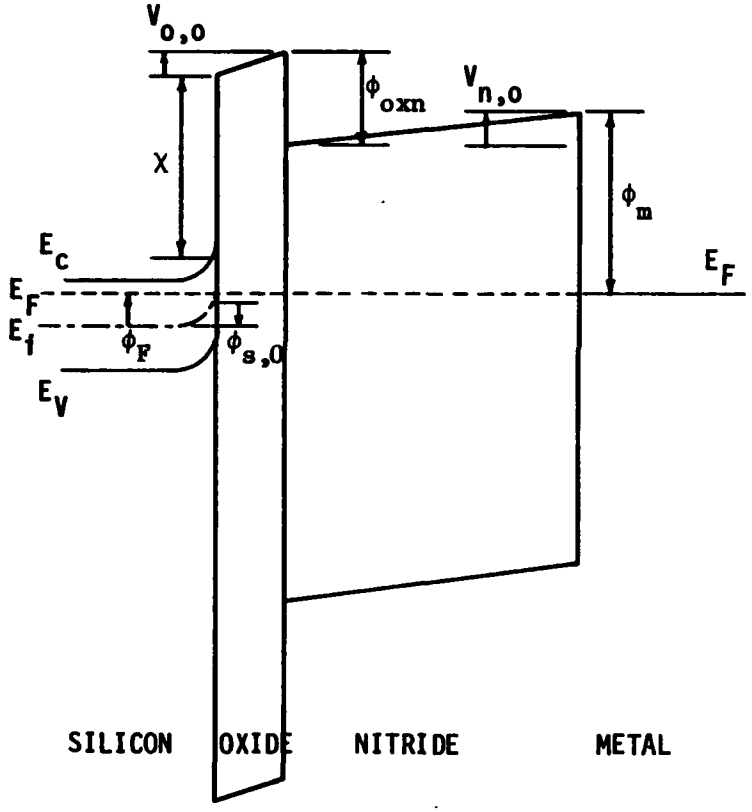
$$V_G = -(Q_{ss} + Q_n + Q_d)/C_{No} + \phi_{ms} + \phi_s \qquad (2.6)$$

where $\frac{1}{C_{No}} \equiv T_{ox}/\varepsilon_{ox} + T_N/\varepsilon_N$

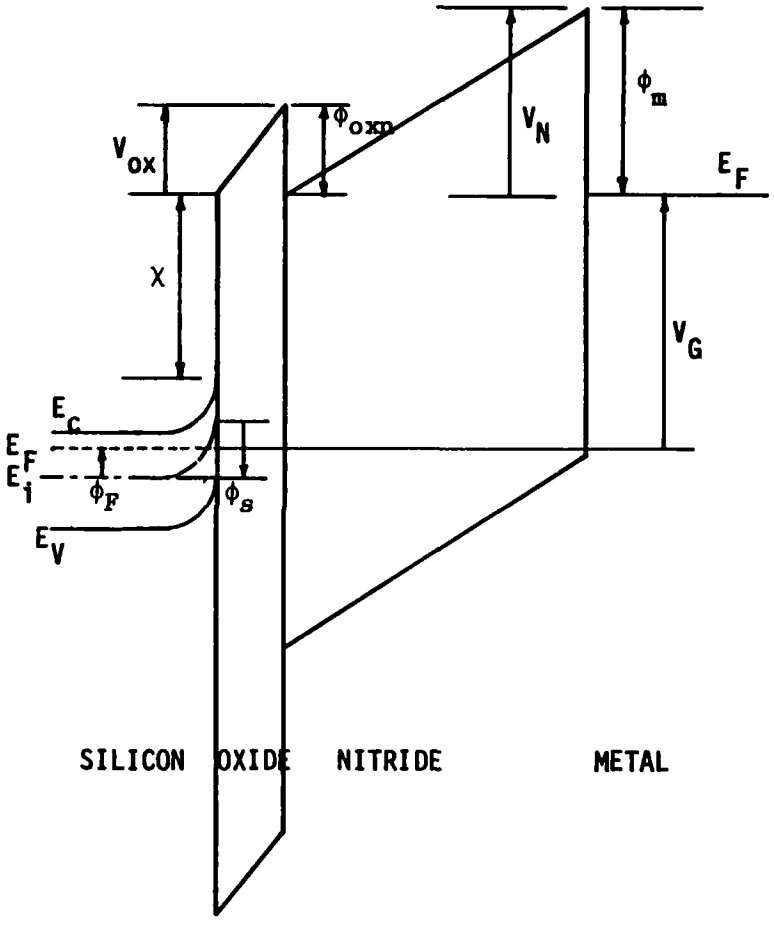
Oxide capacitance/area in series with nitride capacitance/area

Localized charge Q, in the nitride, a distance x from the oxide-nitride interface is shown in Figure 2-6. For zero bias:

$$Q_G + Q_{ss} + Q_n + Q_d + Q = 0$$

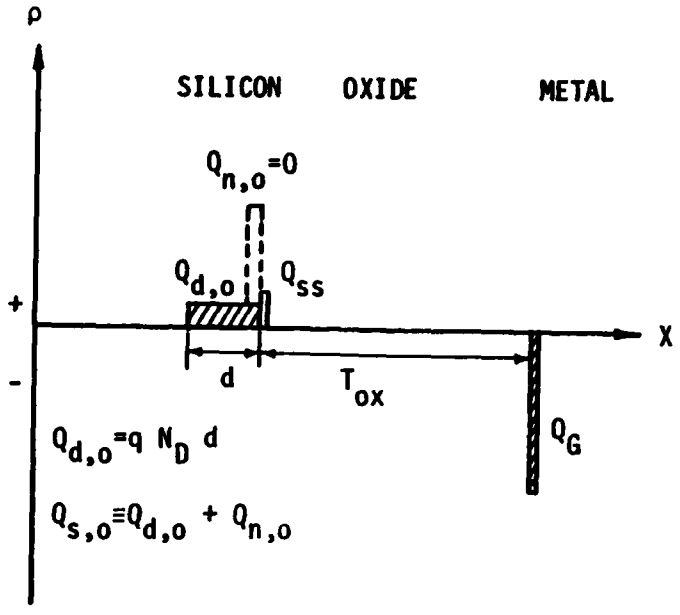


Zero Bias

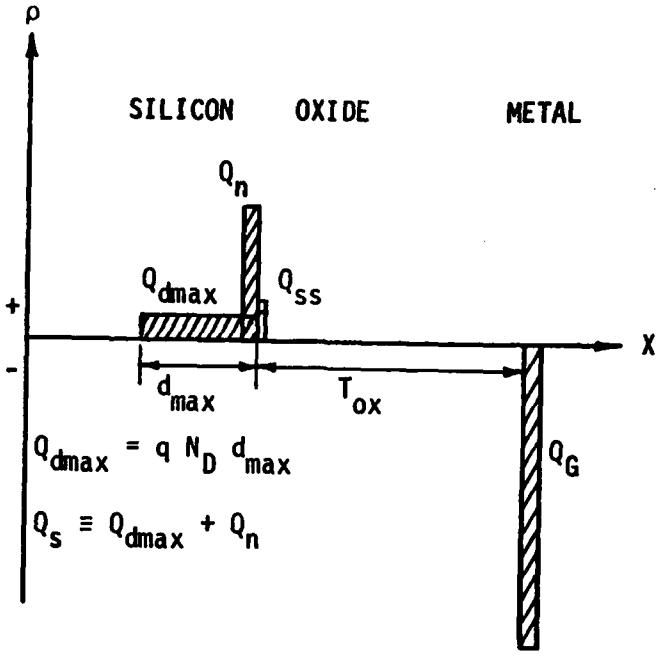


Negative Bias on Metal Gate
(Inversion Condition)

Figure 2-4: MNOS Band Diagrams



Zero Bias



Negative Bias on Metal Gate
(Inversion Condition)

Figure 2-5: MNOS Charge Distribution

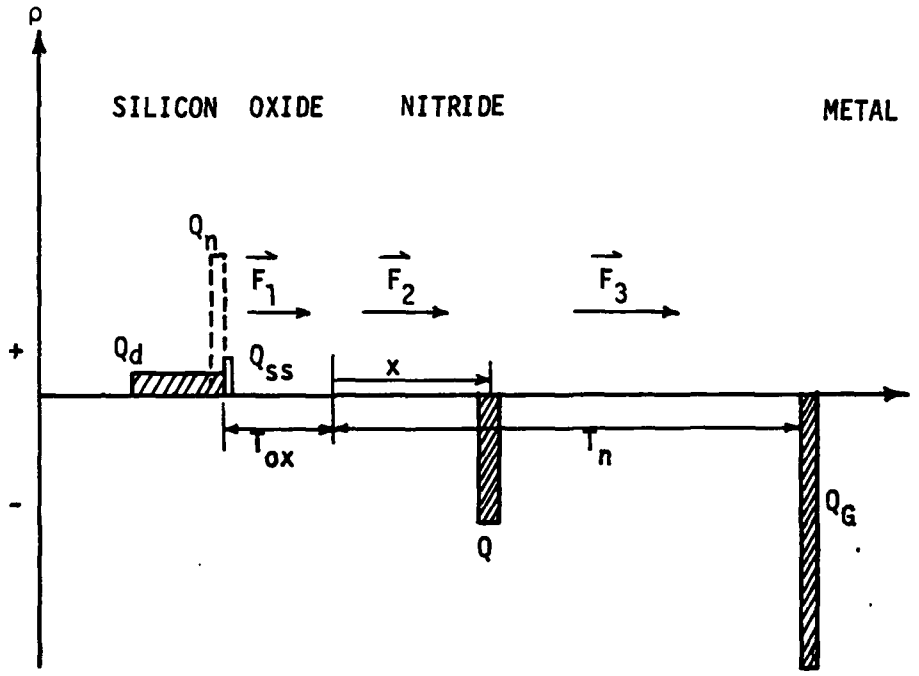


Figure 2-6: MNOS Charge Distribution Including Localized Charge

and

$$0 = V_1 + V_2 + V_3$$

$$= F_1 T_{ox} + F_2 x + F_3 (T_N - x) \tag{2.7}$$

and

$$\varepsilon_{ox} F_1 = \varepsilon_N F_2 \tag{2.8}$$

$$\varepsilon_N (F_3 - F_1) = Q \tag{2.9}$$

From (2.7), (2.8) and (2.9):

$$F_{ox} \equiv F_1 = \frac{Q}{\varepsilon_{ox} \varepsilon_N} (T_N - x) C_{No} \tag{2.10}$$

The induced charge in the semiconductor is:

$$Q_{s \text{ induced}} = -\varepsilon_{ox} F_{ox}$$

Thus, using equation (2.10), the "effective" surface charge then becomes:

$$Q_{eff} = -Q_{s \text{ induced}} = \frac{Q}{\varepsilon_N} (T_N - x) C_{No} \tag{2.11}$$

Adding this Q_{eff} to the naturally occuring Q_{ss} in equation (2.6):

$$V_G = -(Q_{ss} + Q_n + Q_d)/C_{No} - Q(T_N - x)/\varepsilon_N + \phi_{ms} + \phi_s$$

$$= -(Q_{ss} + Q_n + Q_d)/C_{No} - Q(1 - x/T_N)/C_N + \phi_{ms} + \phi_s$$

Consider the charge Q to be localized at the interface. Then $x \equiv 0$ and:

$$V_G = -(Q_{ss} + Q_n + Q_d)/C_{No} - Q/C_N + \phi_{ms} + \phi_s \qquad (2.12)$$

Next, consider the effect of the presence of distributed charge in the nitride, $\rho(x)$, as shown in Figure 2-7. From equation (2.11):

$$dQ_{eff} = \frac{\rho(x)dx}{\varepsilon_N} (T_N - x)C_{No}$$

$$= \rho(x)dx(1 - x/T_N)C_{No}/C_N$$

Thus, adding the total Q_{eff} due to this distributed charge in the nitride to the naturally occuring fixed silicon-silicon oxide interface charge, Q_{ss}, in equation (2.12):

$$V_G = -(Q_{ss} + Q_n + Q_d)/C_{No} - Q/C_N + \phi_{ms} + \phi_s$$

$$+ (T_N C_N)^{-1} \int_0^{T_N} x\rho(x)dx - C_N^{-1} \int_0^{T_N} \rho(x)dx$$

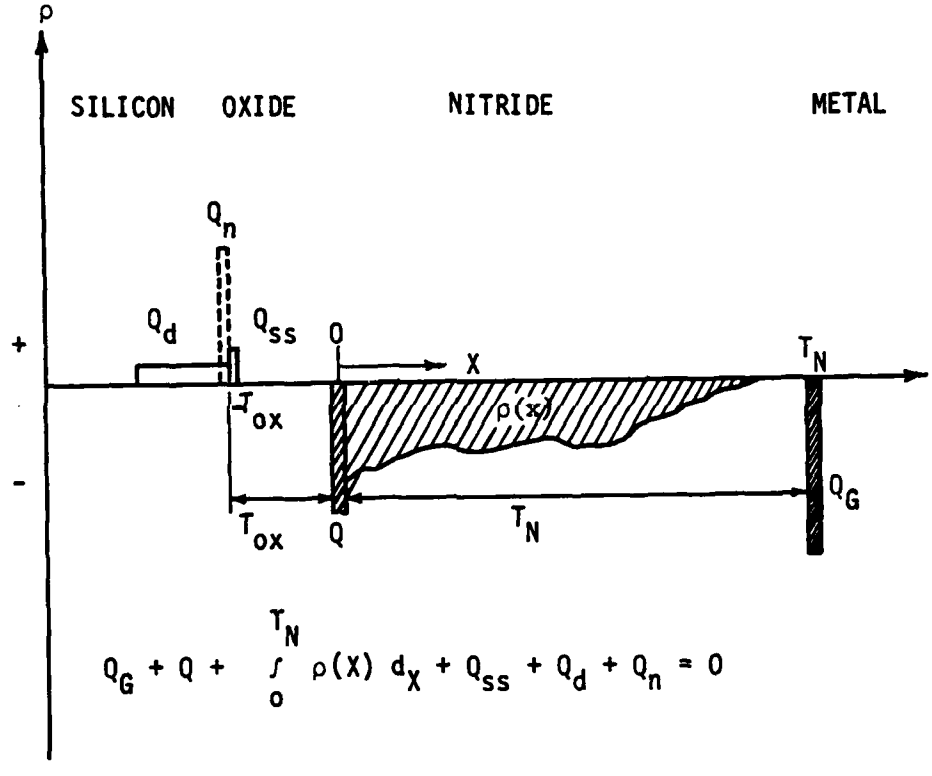


Figure 2-7: Complete MNOS Charge Distribution

From this we get:

$$V_{FB} = -Q_{ss}/C_{No} - Q_T/C_N + (T_N C_N)^{-1} \int_0^{T_N} x\rho(x)dx + \phi_{ms} \qquad (2.13)$$

and

$$V_{TH} = -(Q_{ss} + Q_{dmax})/C_{No} - Q_T/C_N + (T_N C_N)^{-1} \int_0^{T_N} x\rho(x)dx + \phi_{ms} + 2\phi_F \qquad (2.14)$$

where $Q_T \equiv Q + \int_0^{T_N} \rho(x)dx$ = total stored charge.

Assuming a constant Q_{ss}, the only cause for a change in flatband voltage or threshold voltage (as demonstrated by a shift in the C-V curve) is a change in the stored interface or distributed charge since Q_{dmax}, ϕ_{ms} and ϕ_F are all fixed. Note that for any change in stored charge the flatband voltage change is equal to the threshold voltage change.

2.1.2 Charge Centroid Determination

Maes and Van Overstraeten Technique

With X_c, the trapped charge centroid, (distance from the nitride-oxide interface) expressed as:

$$X_c = \int_0^{T_N} \frac{x\rho(x)dx + Q\,x\big|_{x=0}}{Q + \int_0^{T_N} \rho(x)dx} = \int_0^{T_N} \frac{x\rho(x)dx}{Q_T} \qquad (2.15)$$

the flatband voltage of equation (2.13) can be expressed as:

$$V_{FB} = (\phi_{ms} - Q_{ss}/C_{No}) - Q_T(T_N - X_c)/\varepsilon_N \qquad (2.16)$$

The technique proposed by Maes and Van Overstraeten[45, 61] involves flatband voltage measurements on a series of devices, all having "identical" oxide-nitride interface conditions but varying in nitride thickness. This is accomplished by fabricating one large, thick nitride MNOS structure, physically separating it into many small devices, and etching a different thickness of nitride from each device. Each device is charged to the same value of Q_T in the nitride. Therefore from equation (2.16) a plot of V_{FB} vs T_N yields (1) the total charge, Q_T, from the slope and (2) the charge centroid, X_c, from the V_{FB} axis intercept since ϕ_{ms} is known and the Q_{ss} contribution is small and can be ignored for $Q_{ss} < 5 \times 10^{11}$ charges/cm^2.

This method requires selective removal of nitride, electrical determination of flatband voltage, physical measurement of nitride thicknesses, similar interfaces for all devices used and control of device charging to insure stored charge distributions are identical in each device. It then yields the centroid of the total charge within the nitride (the injected charge <u>plus</u> the initial charge before injection). Maes and Van Overstraeten present data indicating that immediately after device fabrication the charge centroid is equal to zero (is at the oxide-nitride interface) and the total stored charge is approximately 10^{12} charges/cm^2. Hence, by using "virgin" devices for each measurement and using data points reflecting charge injection greater than 10^{12} they

were able to demonstrate charge penetration into the nitride.

This technique also requires that the charge distribution in the nitride (Q and $\rho(x)$) is the same for all devices. To achieve this, Maes and Van Overstraeten invoke the Lundstrom and Svensson development[24] in which the steady state charging condition is controlled by an oxide electric field-dependent oxide current and a nitride electric field-dependent nitride current. Maes and Van Overstraeten develop expressions for initial nitride field as a function of gate voltage and constant initial nitride stored charge, and for oxide field as a function of nitride field, nitride stored charge, centroid and nitride thickness.

$$F_{ox}(t) = (\varepsilon_N/\varepsilon_{ox})F_{N0} + [Q_T(t)/\varepsilon_{ox}](1 - X_c/T_N)$$

At $t = 0$ the stored charge, $Q_T(0)$, is the same for the differing thickness devices and the centroid is zero. Therefore, for identical initial nitride fields, the oxide and nitride currents (as determined solely by the oxide and nitride fields) in all devices are equal, creating identical injection conditions. They then state that this will cause the initial charge storage distributions to be identical. They assume the charge centroid remains much less than the nitride thickness, hence the oxide electric field will not vary much with nitride thickness. They also neglect any nitride field change with changing stored charge. They then conclude that all these conditions will lead to a steady state charge distribution (Q and $\rho(x)$) that is identical in all devices.

Yun Technique

The technique proposed by Yun[44, 10] involves two simultaneous electrical measurements: flatband voltage shift and total integrated current through the MNOS device while a sufficiently large gate pulse is applied to inject charges into the device. By conservation of charge, the integrated current through the device, J, is composed of the conduction current in the nitride adjacent to the metal gate, J_N, the change in charge stored in the insulators (nitride, nitride-oxide interface and oxide), $\Delta q_i(t) \equiv q_i(t) - q_i(0)$, and the change in charge in the oxide-silicon interface states and the silicon depletion layer, $\Delta Q_S(t) \equiv Q_S(t) - Q_S(0)$.

$$Q(t) \equiv \int J(t)dt = \int J_N(t)dt - \Delta q_i(t) - \Delta Q_S(t) \qquad (2.17)$$

The contribution to Q(t) of $J_N(t)$ is negligible if the applied pulse amplitude is low enough and duration is short enough that charge injected from the silicon can not reach the gate or recombine with any charge injected from the gate which would cause J_N. The contribution of $\Delta Q_S(t)$ can be zero if $Q_S(t) = Q_S(0)$. This will be the situation if the silicon surface potential $\phi_s(t)$ is made equal to $\phi_s(0)$, since then the surface state occupancy will be the same and the depletion layer charge configuration will also be the same.

The total MNOS capacitance is the fixed nitride capacitance, $C_N = \epsilon_N/T_N$, the fixed oxide capacitance, $C_{ox} = \epsilon_{ox}/T_{ox}$, and the silicon

capacitance (determined by the depletion layer capacitance) in series. Maintaining the total MNOS capacitance at a constant value would thus insure that the silicon surface conditions (interface states and ϕ_s) remain constant and hence $\Delta Q_s(t) = 0$ for all times. The result is that equation (2.17) reduces to:

$$Q(t) = -\Delta q_i(t)$$

Therefore, since it is assumed that there is no charge trapping in the thin oxide layer, the net stored charge in the bulk nitride and nitride-oxide interface can be measured by obtaining the total integral of the current passing through the device while it is pulsed and while the surface potential is returned to its value before the pulse.

During the centroid measurement process the device C-V curve and operating point vary as shown in Figure 2-8. The device is initially biased with V_{start} and exhibits a capacitance $C_{MNOS}(1)$. Following a write pulse the C-V curve shifts to the new position because of charges injected into and trapped in the device. The device capacitance changes to $C_{MNOS}(2)$, reflecting the existing bias voltage, V_{start}, and the shifted C-V curve. The bias voltage is then changed to V_{new} which causes the capacitance to change to $C_{MNOS}(3) = C_{MNOS}(1)$. It is apparent that the required ΔV_{bias} is the same as the flatband voltage shift, ΔV_{FB}, due to the stored charge injected into the nitride by the write pulse.

Repeating the general expression for flatband voltage as developed

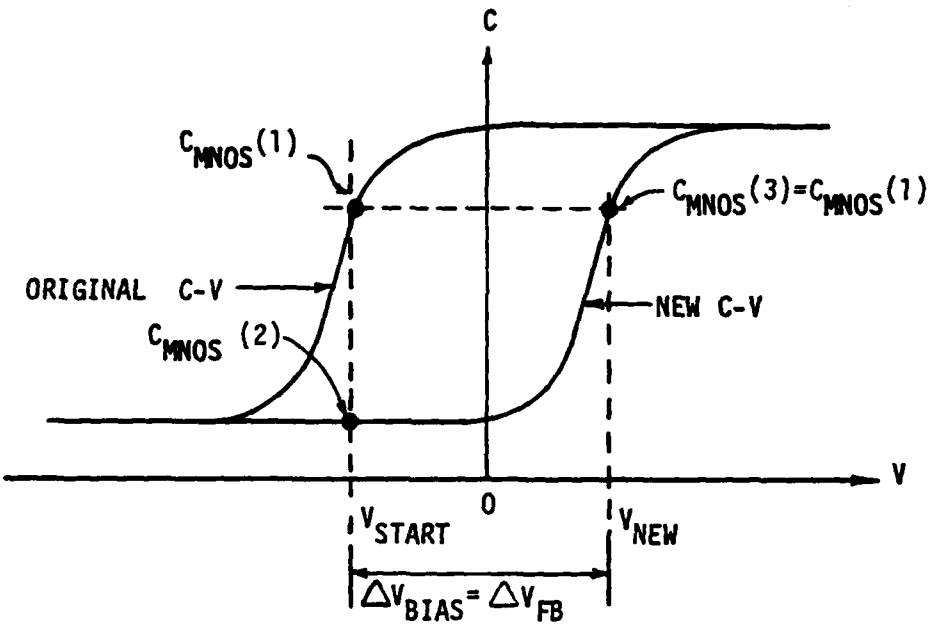


Figure 2-8: Centroid Measurement C-V Curves

in equation (2.13).

$$V_{FB}(t) = -Q_{ss}/C_{No} - C_N^{-1} \int_0^{T_N} \rho(w,t)dw$$

$$+ (T_N C_N)^{-1} \int_0^{T_N} w\rho(w,t)dw + \phi_{ms}$$

where w = distance from oxide-nitride interface
$\rho(w)$ = total charge distribution (interface plus bulk nitride charges)

Rewriting the above using x = the distance from the gate as a parameter:

$$V_{FB}(t) = -Q_{ss}/C_{No} - (T_N C_N)^{-1} \int_0^{T_N} x\rho(x,t)dx + \phi_{ms} \qquad (2.18)$$

From equation (2.18) the following expressions relating the change in flatband voltage, $\Delta V_{FB}(t) \equiv V_{FB}(t) - V_{FB}(0)$, to the change in charge distribution can be shown:

$$\Delta V_{FB}(t)\varepsilon_N/Q(t) = Q(t)^{-1} \left[-\int_0^{T_N} x\rho(x,t)dx - \left(-\int_0^{T_N} x\rho(x,0)dx\right)\right] \qquad (2.19)$$

where:

$\rho(x,0) = \rho_0(x,0)$ = the initial charge distribution

$\rho(x,t) = \rho_0(x,t) + \rho_g(x,t) + \rho_s(x,t)$

= the redistribution of the initial charge plus the charge distribution due to injection into the nitride from the gate and from the silicon (through the oxide)

Consideration of the energy levels and electric fields concerned indicates that for a large positive pulse, injection of large numbers of electrons from the silicon conduction band through the oxide is more probable than injection of quantities of holes from the gate. Additionally, the injected electrons, being closer to the silicon surface, are more heavily weighted in their contribution to the flatband voltage shift. Hence, $\rho_g(x,t)$ can be neglected.

Forming the charge centroids and total charge expressions required to rewrite equation (2.19):

$$\Delta q_i(t) = \int_0^{T_N} \rho_S(x,t)dx$$

$$X_S \equiv \frac{\int_0^{T_N} x\rho_S(x,t)dx}{\int_0^{T_N} \rho_S(x,t)dx} = \int_0^{T_N} \frac{x\rho_S(x,t)dx}{\Delta q_i(t)}$$

$$q_0 \equiv \int_0^{T_N} \rho_0(x,0)dx = \int_0^{T_N} \rho_0(x,t)dx$$

$$\delta_0 \equiv X_0(t) - X_0(0) = \int_0^{T_N} x\left[\frac{\rho_0(x,t)}{q_0} - \frac{\rho_0(x,0)}{q_0}\right]dx$$

Substituting the above into equation (2.19) and using $Q(t) = -\Delta q_i(t)$:

$$V_{FB}(t)\ \varepsilon_N/(-\Delta q_i(t)) = -\ (\Delta q_i(t))^{-1}\ [-\Delta q_i(t)\ X_S - q_0\ \delta_0]$$

or

$$\frac{\varepsilon_N \Delta V_{FB}(t)}{Q(t)} = X_S[1 + q_0\delta_0/(\Delta q_i(t)\ X_S)] \qquad (2.20)$$

It is assumed that during the short write pulses for which the nitride current, J_N, is negligible, the initial charge distribution is not altered appreciably by application of the pulse, and hence $\delta_0 << X_S$. That it is reasonable to neglect the δ_0 term can also come from considering that the initial distribution is nearly all trapped charge (very few free charges in the nitride insulator). Therefore, δ_0 must be small since it essentially arises only from trapped charge movement by conduction through the nitride which requires detrapping, charge flow and retrapping. The value X_S arises from the charge injected from the silicon, thus X_S can be expected to be in the range $X_S = T_N/2$ to T_N (ie. closer to the nitride-oxide interface than to the gate electrode). Thus again, $\delta_0 << X_S$. In addition, if the device is initially adjusted such that $C_{MNOS}(V_{bias} = 0) = C_{FB}$ then the net initial stored charge, q_0, is nearly equal to zero and definitely small with respect to Δq_i. This causes the ratio term in the right hand side of equation (2.20) to be negligible compared to 1.

Thus the distance <u>from the nitride-oxide interface</u> to the centroid of the injected charge is given by the expression:

$$X_c = T_N - X_S = T_N - \varepsilon_N \Delta V_{FB}(t)/Q(t) \qquad (2.21)$$

Using this technique, Yun[44] has found the centroid to be as much as one third the way across the nitride in conventional thin oxide MNOS devices.

2.2 Experimental Equipment and Analysis Procedure

2.2.1 Measurement Equipment

System Configuration

The centroid measurement system shown in Figure 2-9 was composed of circuitry to measure the total charge injected into an MNOS device and the corresponding flatband voltage, gate bias and write voltage pulse sources; an oscilloscope to observe initial conditions of circuit prior to application of write pulse; an X-Y recorder for analog recording of injected charge and flatband voltage as a function of time; a multichannel voltage scanner to sample and digitize injected charge signal and flatband voltage; and a calculator, a printer and an X-Y plotter to store, analyse, calculate and plot the charge centroid, injected charge and flatband voltage as a function of time after write pulse. A detailed circuit diagram of the centroid circuitry is shown in Figure 2-10.

Centroid Circuitry Operation

To describe the operation of the centroid circuitry the simplified charge centroid circuitry of Figure 2-11 is used. The instantaneous

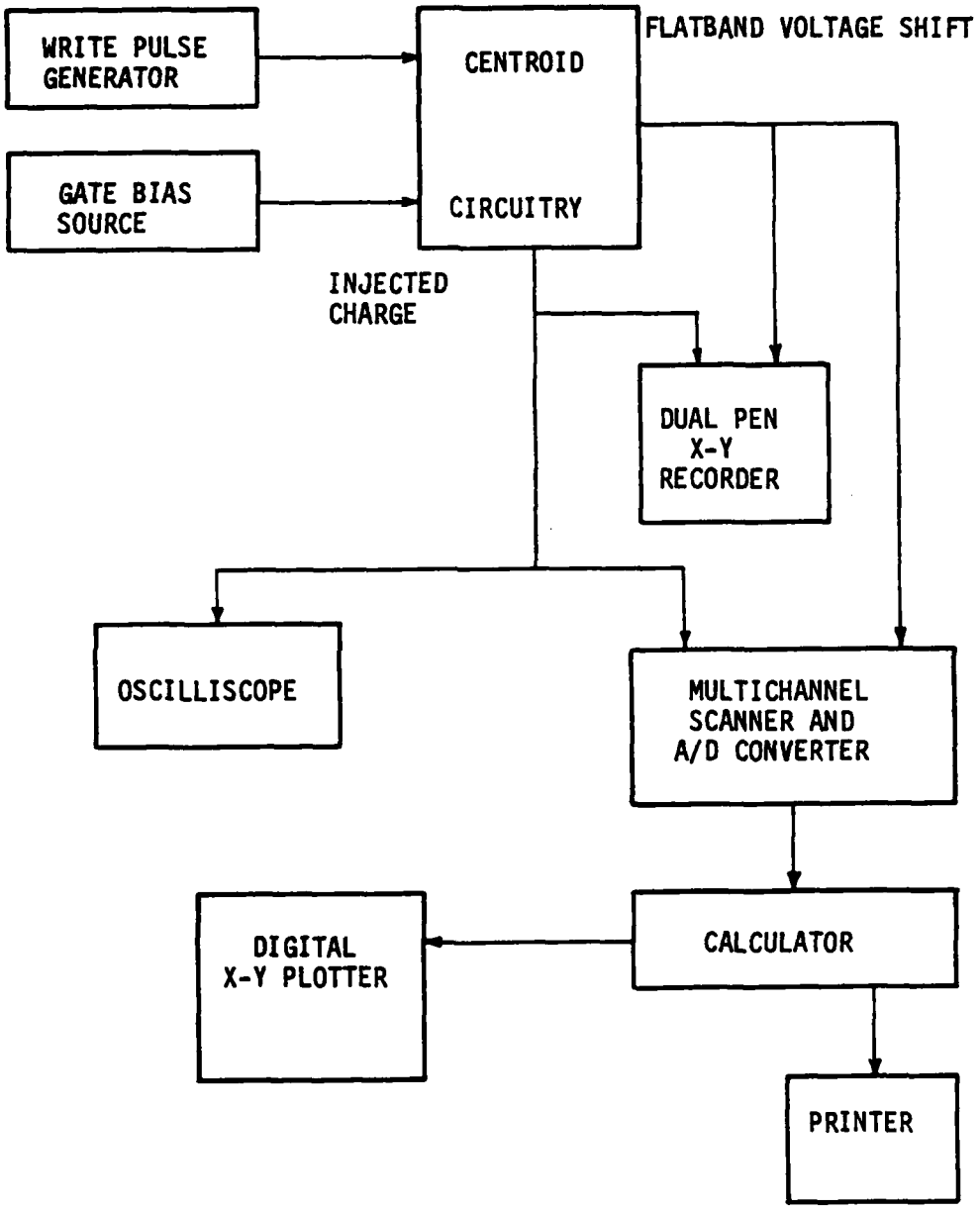


Figure 2-9: Charge Centroid System

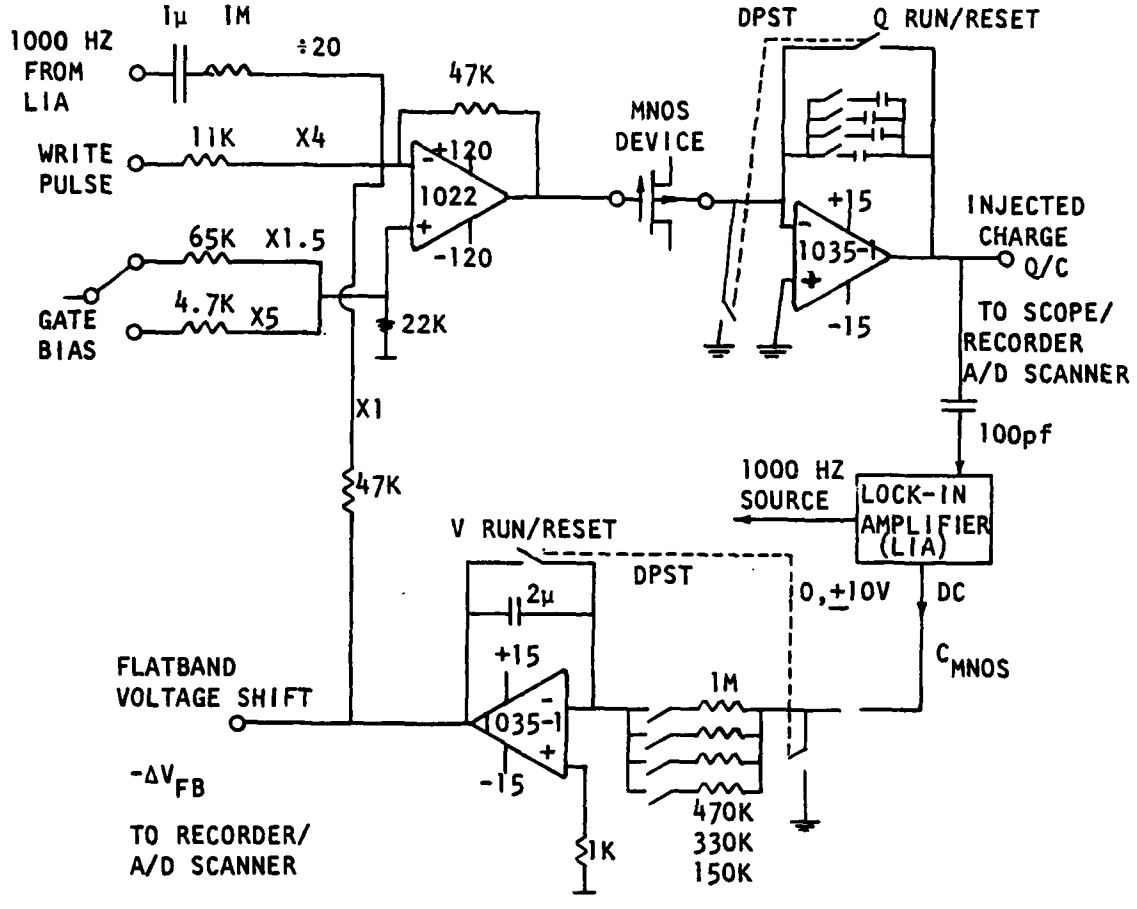


Figure 2-10: Detailed Charge Centroid Circuitry

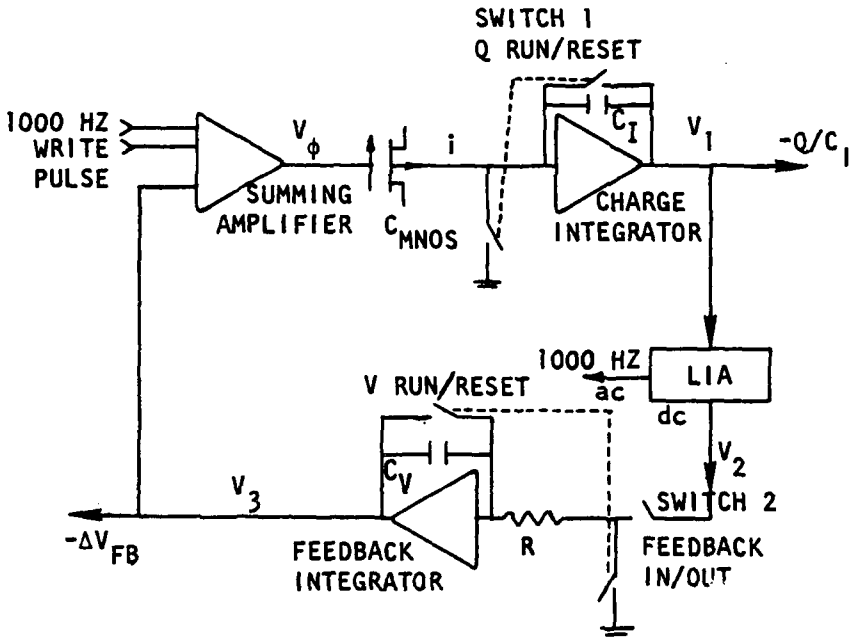


Figure 2-11: Simplified Charge Centroid Circuitry

capacitance of the MNOS device was determined using a lock-in-amplifier(LIA). The LIA was set to provide a reference frequency of 1000 Hz. This ac signal was attenuated such that only 15 mV was applied to the test device, assuring that no capacitance change could result from this applied measurement signal. The amplitude of the ac current through the MNOS device, and entering the charge integrator, is proportional to the MNOS capacitance. The ac voltage out of the charge integrator and detected by the LIA is proportional to the ratio of the MNOS capacitance to the integrator capacitor value, C_{MNOS}/C_I. The dc output of the LIA is proportional to the input ac amplitude, and hence to the MNOS capacitance. The LIA has the feature of variable output offset. This permits adjustment of the output voltage to zero for a specific MNOS capacitance condition and then any subsequent increase or decrease in MNOS capacitance is reflected in a positive or negative output voltage swing. Although the absolute value of MNOS capacitance is not needed for the centroid measurement system, the experimental setup was checked for accuracy over the 10 to 1000 picofarad range by substituting fixed capacitors, measured on a calibrated capacitance meter, for the MNOS device. The output of the LIA reflected the measured capacitance with less than a 3 percent error.

With switch 2, Feedback In/Out, open and switch 1, Q Run/Reset, open (RUN position), the dc output of the LIA will indicate the capacitance of the MNOS device. The LIA output offset can then be set to cause a zero volt output for this value of MNOS capacitance. When a write pulse is applied to the MNOS device through the summing amplifier, the charge integrator output, V_1, reflects the charge motion through the

device.

$$V_1 = -(C_I)^{-1} \int i(t)\, dt = -Q/C_I$$

The resulting capacitance change of the MNOS device is indicated by the non-zero dc output, V_2, of the LIA.

With switch 3, V Run/Reset, open (RUN position), closing switch 2 causes V_2 to be applied to the feedback integrator. The output of the integrator, V_3 is applied to the MNOS device through the summing amplifier. V_3 will continue to change as long as the LIA output, V_2, is non-zero.

$$V_3 = -(RC_v)^{-1} \int V_2(t)\, dt$$

This feedback voltage, applied as a bias voltage, shifts the MNOS capacitance back to its before-the-pulse value causing the dc output of the LIA, V_2, to return to zero, stabilizing the value of V_3, the flatband or threshold voltage shift.

Thus the requirement of restoring the MNOS device to its initial capacitance value (initial ϕ_s and silicon charge distribution conditions) is performed automatically, causing the output, V_1, of the charge integrator to reflect the change in charge stored in the MNOS device caused by the write pulse.

Centroid Circuitry Design Considerations

The reset position of the switch lebeled "Q Run/Reset" discharges the integrator before each run and also allows the MNOS device to be erased while still in the circuit, with an opposite polarity pulse of extended duration, without over-driving the charge integrator. Switchable values of C_I were used in order to obtain maximum values for V_1, yet still stay within the operating range of the op-amp, for MNOS devices having various cross section areas and for various write pulse conditions. The reset position of switch V Run/Reset discharges the integrator before each run. Switchable values for R were used to optimize the response time of the feedback loop while preventing oscillations under various conditions of capacitance change (large and small V_2). The Philbrick model 1035-1 op-amp was used for both integrators due to having a low (<0.1 picoamp) input bias current which is needed for an accurate integrator. The drift of the feedback integrator due to input bias current was negligible (<0.5 mV/min) compared to the flatband voltage shifts encountered during centroid measurements. This input bias current caused drift of the charge integrator in the range of 20 to 80 mV/min which resulted in a contribution to V_1 that was on the order of that due to the MNOS injected charges for small devices and low, short write pulses. This effect was accounted for by taking data before each run representing the bias current effect and automatically calculating and applying a correction factor during data analysis by the calculator. A Philbrick model 1022 op-amp was used for the summing amplifier because it has a

±140 volt operational range and 30 volt/microsecond rise time which would accomodate all anticipated write/erase pulse conditions.

Typical Output Curves

Examples of typical analog X-Y traces of large injected charge, large flatband voltage shift and small injected charge, small flatband voltage shift measurements resulting from write pulse application at a time t_1 are shown in Figures 2-12 and 2-13. The silicon charge redistribution when the surface potential and depletion layer charge are returned to their initial conditions by application of the feedback bias (ΔV_{FB}) at time t_2 is very obvious in the Q/C_I curve.

The effect of the charge integrator op-amp input bias current on the injected charge measurement is easily seen in Figure 2-13. Overshoot of ΔV_{FB} when initially applied at t_2 and subsequent minor oscillation can also be seen.

2.2.2 Analysis Procedure

A program was written for an HP9820 calculator to automatically input and store the sampled, digitized flatband voltage shift (ΔV_{FB}) and injected charge (Q/C_I) data. After the data acquisition a printout of the raw data is produced and the values of C_I, nitride thickness and MNOS device area are entered. The calculator is used to locate the time instants t_1 and t_2, determine the value of measurement system zero drift of ΔV_{FB} at t_2 and of Q/C_I at t_1 and subtract this from the raw data values. The Q/C_I data prior to t_1 is then used to automatically calculate the dV/dt due to the integrator input bias current. This is

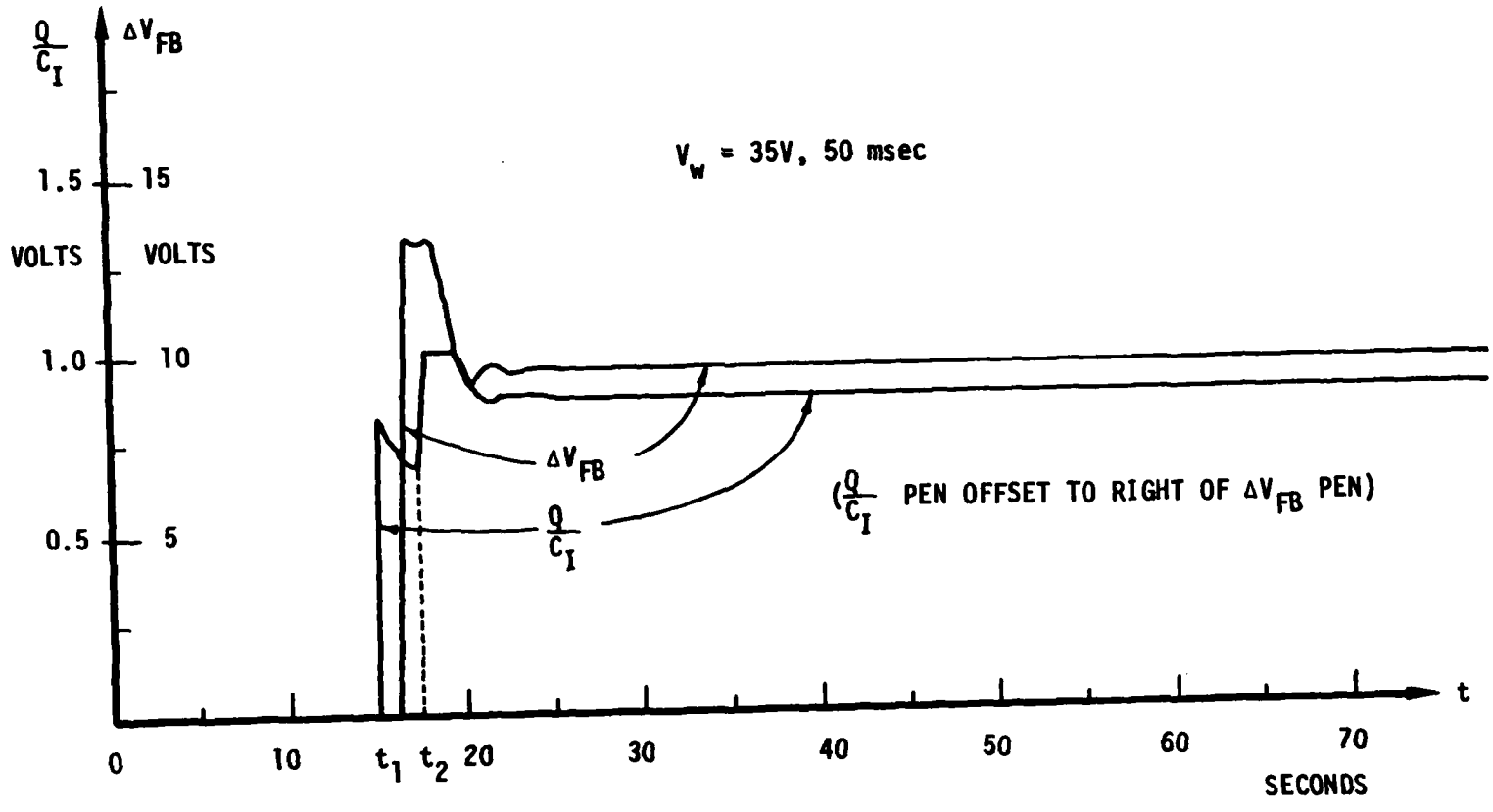


Figure 2-12: Large Magnitude Injected Charge and Flatband Voltage Shift

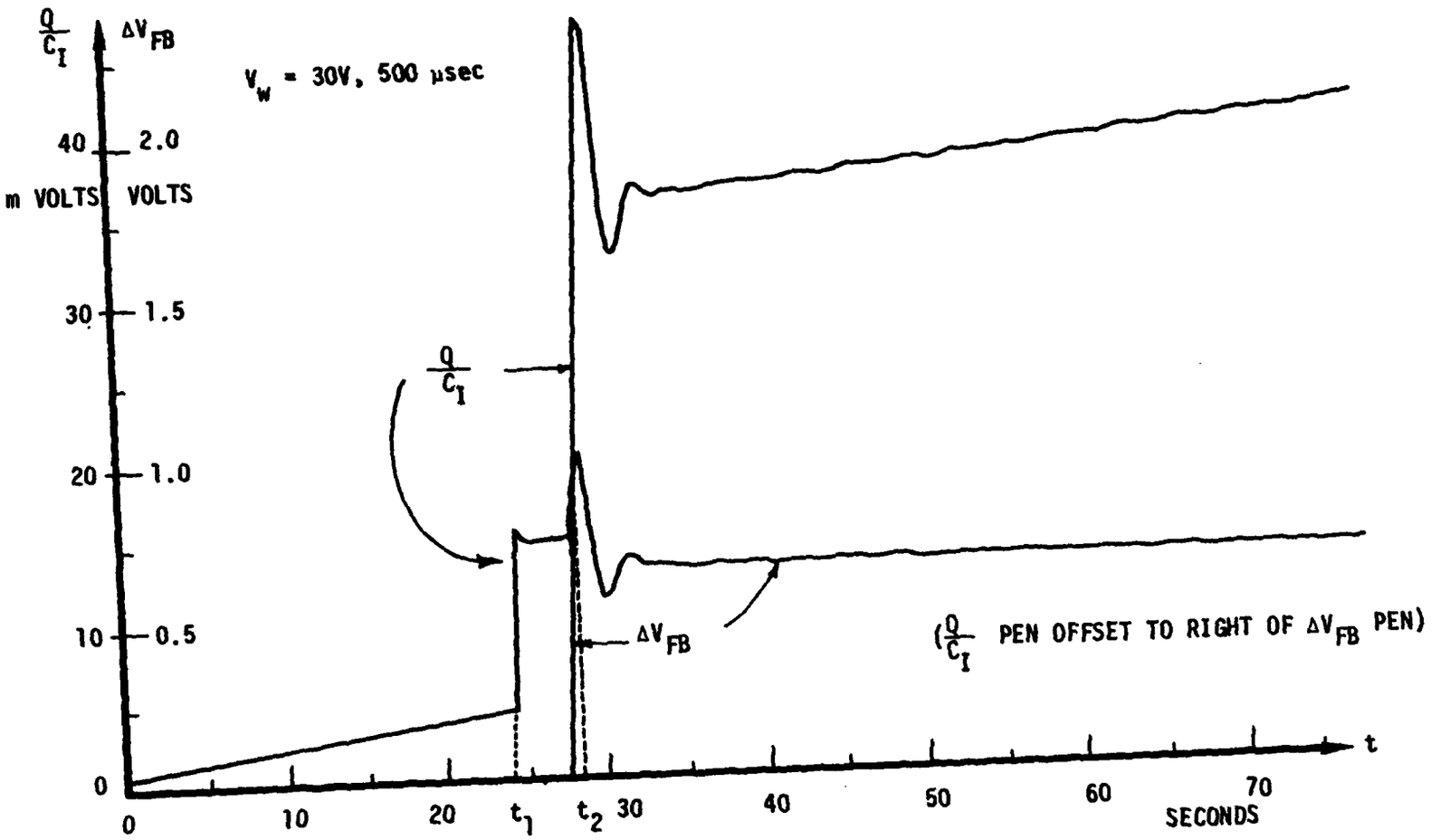


Figure 2-13: Small Magnitude Injected Charge and Flatband Voltage Shift

then applied as a final correction factor to the Q/C_I data.

The corrected ΔV_{FB} and Q/C_I data points after t_2 are examined to locate a point in the region where the data first "flattens out". This point will thus be just beyond any short period of overshoot or oscillation in ΔV_{FB} that might have occurred while returning the MNOS device to its initial capacitance value and before any drift in the Q/C_I curve due to integration capacitor discharge. The values of ΔV_{FB} and Q/C_I are then used in equation (2.21) to calculate the charge centroid. This calculated value of centroid plus the other parameters required for equation (2.21) are then printed out.

The corrected values of ΔV_{FB} are plotted as a function of time on the digital X-Y plotter. The values of Q/C_I are converted to charge/area, Q/A, values and are plotted as a function of time on the digital X-Y plotter.

Using the corrected values of ΔV_{FB} and Q/A after t_2 a point-by-point calculation of charge centroid, X_c, as a function of time is performed. The results of these calculations are printed and then plotted as a function of time.

2.3 Results

The devices used for charge centroid measurements were 165 mil^2 metal-insulator-semiconductor (MIS) capacitor structures fabricated [65] on 5 ohm-cm, n-type, (100), silcon substrates with aluminum as the insulator metalization. The thin thermal oxide was grown at 1050° C in one percent oxygen in argon. The tungsten interface dopant was deposited by electron beam evaporation. Dopant density of these

monolayer range films was controlled by a quartz crystal thickness monitor which had been calibrated by deposition and accurate measurement of tungsten films approximately 100 monolayers thick. The nitride was deposited in an rf heated reactor at 850° C by the reaction of ammonia and silane. The NH_3:SiH_4 ratio was 1000:1. The device chips were mounted in dual in line packages. The nitride and oxide thickness and tungsten dopant density parameters for the four types of devices measured are shown in Table 2-1.

	Nitride Thickness (angstroms)	Oxide Thickness (angstroms)	Tungsten Density (number/cm^2)
A	468	32	None
B	515 *	32	0.3×10^{15}
C	468	32	2.0×10^{15}
D	468	52	0.3×10^{15}

* See Page 78

Table 2-1: Device Parameters

In order to obtain centroid versus injected charge data, write pulses of 10 microseconds through 50 milliseconds duration and 20 to 35 volt amplitude were used. Measured injected charge ranged from 0.6×10^{11} to 2.7×10^{13} charges/cm^2.

2.3.1 Automated Analysis Data

Figures 2-14 and 2-15 show typical digitized plots of injected charge, flatband voltage shift and centroid as a function of time for high and low levels of injected charge. Figure 2-16 is a plot of data from a run during which the nitride current at the gate contact, J_N, was

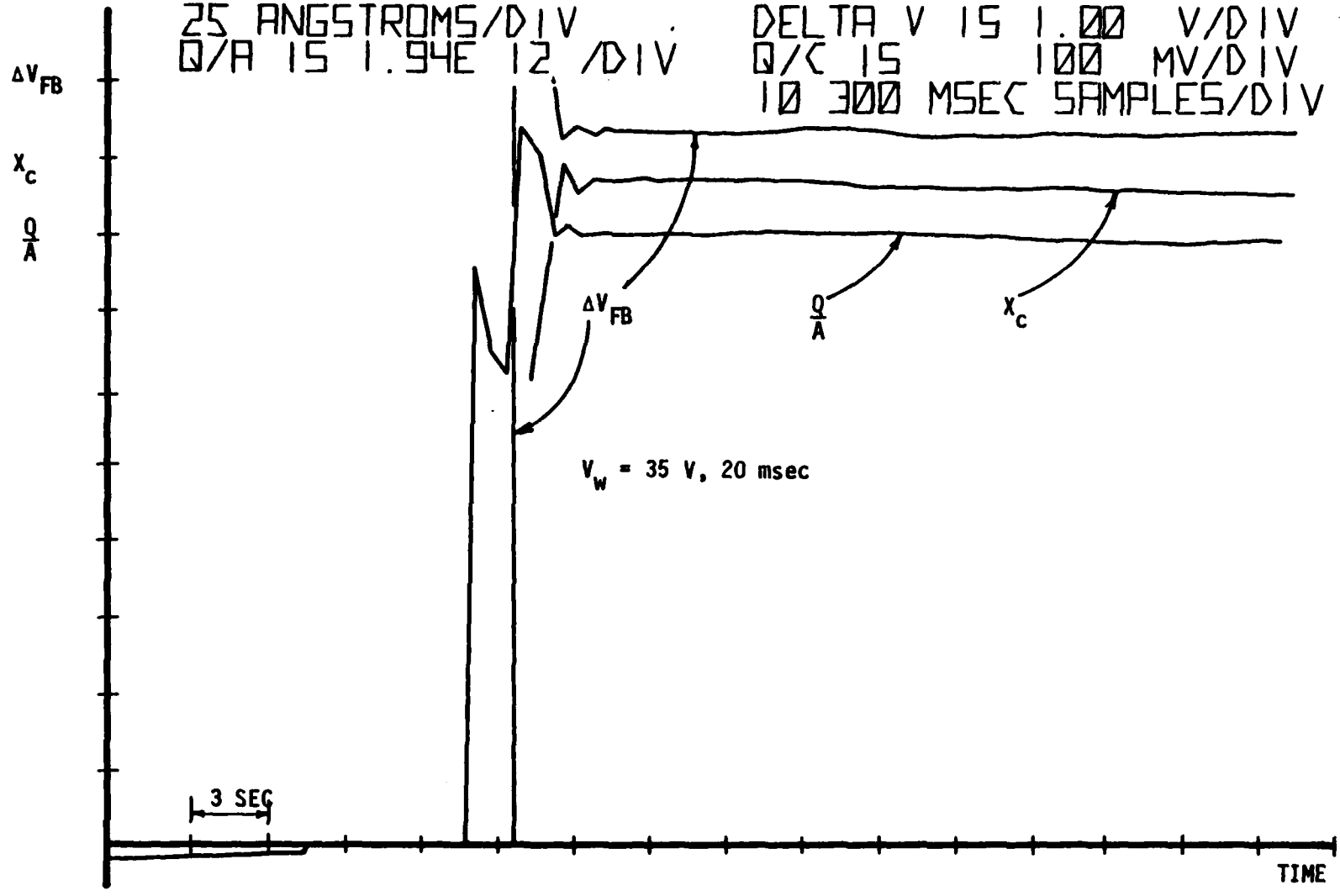


Figure 2-14: Data Plot: High Injected Charge Level

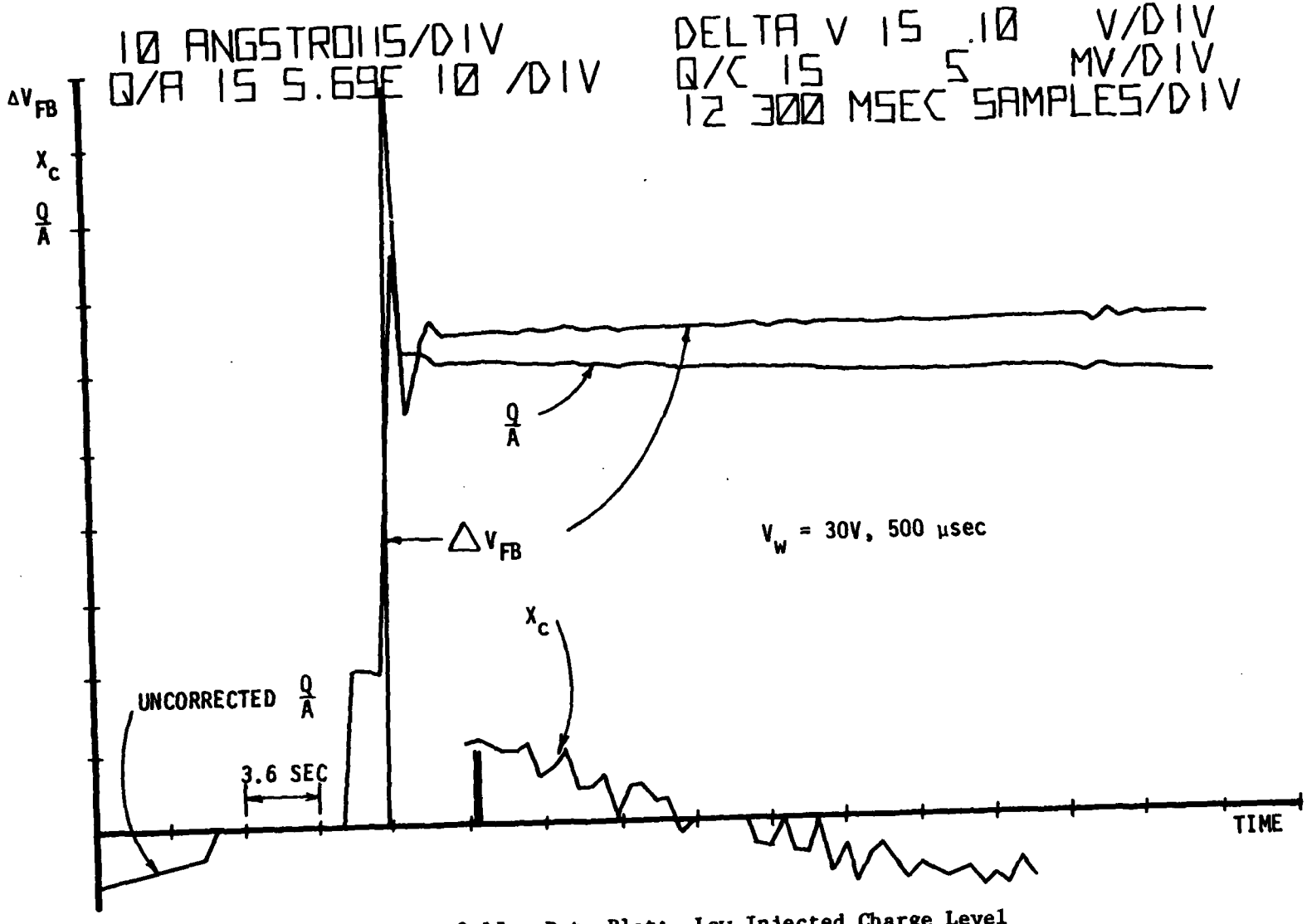


Figure 2-15: Data Plot: Low Injected Charge Level

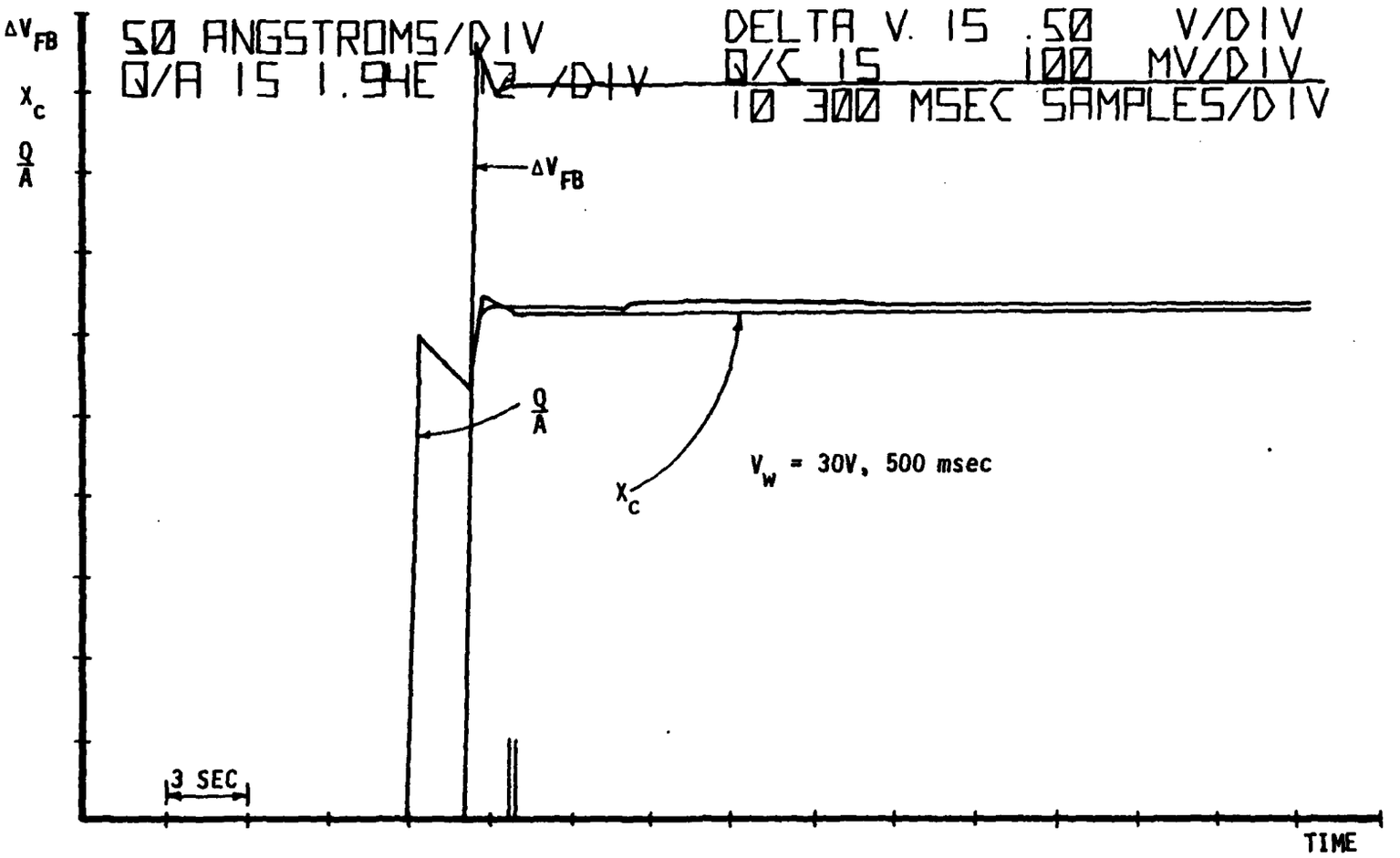


Figure 2-16: Data Plot: J_N Not Negligible

not negligible. In this case the measured Q/C from the current integrator is greater than the actual stored charge leading to an unrealistic centroid that is calculated (equation (2.21)) to be much deeper than half the nitride thickness.

The noticible drift in the Q/A curves of Figures 2-14 and 2-15 is attributed to capacitor discharge by excess current leakage through the circuitry surrounding the integrator, specifically, leakage through the ganged switches controlling the value of integration capacitance, the double pole-single throw switch controlling the Q Run/Reset function and the interconnect wiring. The magnitude of the drift (0.18 to 0.36 millivolts/second) implies a discharge current of 0.6 to 1.2 picoamps for the 3300 picofarad capacitance used for these experiments. Considering the respective voltages on the integrator capacitance of 0.01 to 0.4 volts, discharge resistances are in the range of 0.2 to 3.0×10^{10} ohms. These effects enter into the analysis technique for determining what values of ΔV_{FB} and Q/A to use to calculate X_c (Section 2.2.2).

2.3.2 Injected Charge versus Charge Centroid Data

Conventional (No Dopant) Device:

Injected charge versus centroid characteristics were measured on ten conventional (no interface dopant) MNOS capacitors (type A in Table 2-1). As many as ten runs were made on individual devices. From the data analyses of these devices the plot of Injected Charge versus Charge Centroid of Figure 2-17 was constructed. The data indicated by

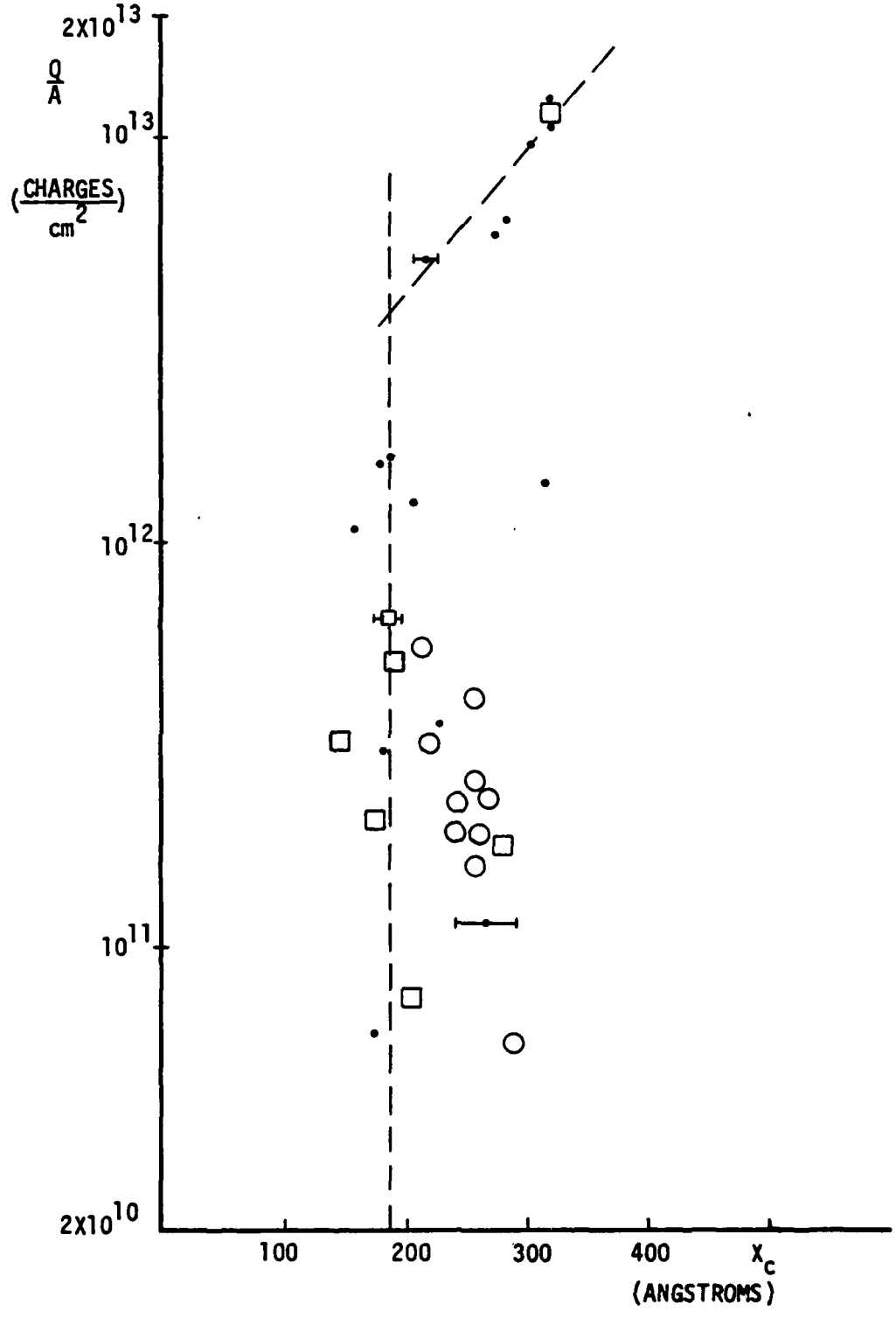
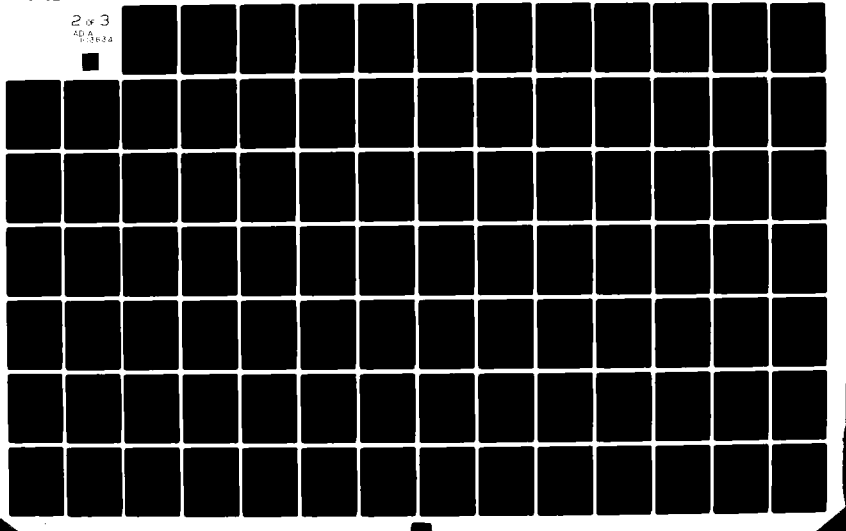


Figure 2-17: Injected Charge vs Centroid - No Dopant

AD-A103 634 AIR FORCE INST OF TECH WRIGHT-PATTERSON AFB OH SCHOO--ETC F/G 9/1
CHARGE TRAPPING IN INTERFACE DOPED MNOS STRUCTURES.(U)
JUL 81 W G SUTTON

UNCLASSIFIED AFIT/DS/EE/81-2 NL



squares came from one device, that by circles from a second, and the remaining data points are the results of measurements on eight other devices. The system noise, evident in Figure 2-15, contributes errors to the calculated centroid indicated by the error bars through points representative of low, medium and high injected charge conditions.

This injected charge versus centroid relationship indicates that even under relatively low charge injection conditions the charge is stored throughout the nitride of a conventional MNOS device. The average of the values of centroid shown in Figure 2-17 for charge injection below 5.5 x $10^{11}/cm^2$ is 220 angstroms. This is just less than the midpoint of the 468 angstrom nitride indicating a fairly uniform charge trapping throughout the nitride.

Thin Oxide, Low Dopant Density Device:

From the data analyses of 16 runs on three devices with thin oxides and low interface dopant density (type B in Table 2-1) the plot of Injected Charge versus Charge Centroid of Figure 2-18 was constructed. Error bars for representative points are shown. For this set of devices the value of nitride thickness used in the data analyses (468 angstroms) resulted in calculations of negative charge centroid, that is, it appeared that the centroid was "behind" the oxide-nitride interface in the oxide or the silicon. Subsequent to the data analyses it was found that the nitride was very uneven across the wafer used for these devices. The edge region of the wafer from which these devices were obtained was thicker than the center portion from which the nitride

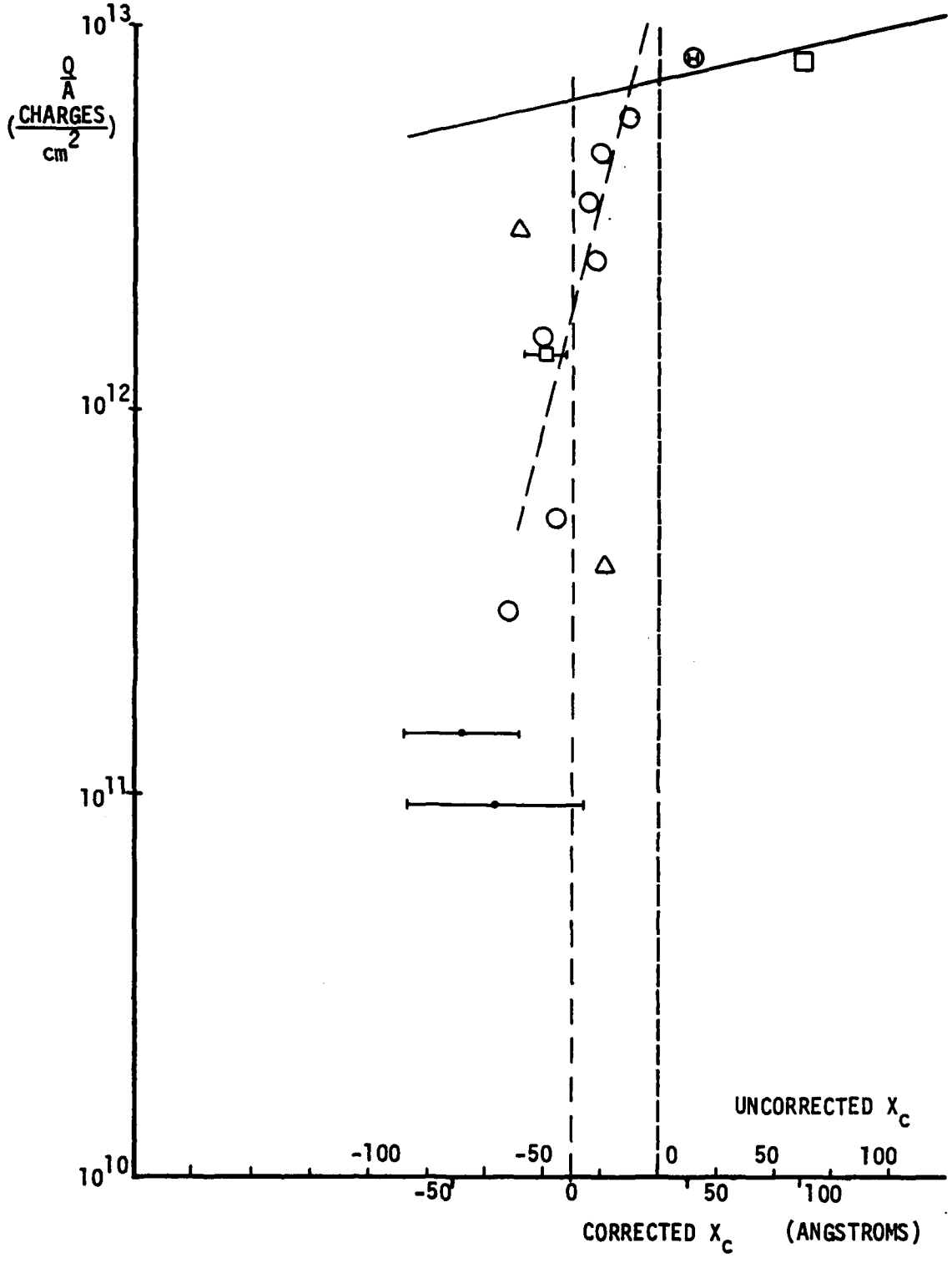


Figure 2-18: Injected Charge vs Centroid - Thin Oxide, Low Dopant Density

thickness measurement was derived. Based on the centroid data the nitride thickness is 515 angstroms. The corrected centroid scale is also noted on Figure 2-18.

Thin Oxide, High Dopant Density Device:

As part of the experiments on these devices (type C in Table 2-1) an extensive series of charge centroid runs were made on one of the thin oxide, high dopant density devices to demonstrate more fully (1) localized charge trapping at the dopant induced sites at the oxide-nitride interface, (2) interface trap filling saturation, and (3) subsequent penetration of charge throughout the nitride. The result of this series is shown in the plot of Injected Charge vs Charge Centroid of Figure 2-19. Error bars for representative points are shown.

Thick Oxide, Low Dopant Density Device:

To examine the effect of oxide thickness variation on charge trapping characteristics, thick oxide, low dopant density devices (type D in Table 2-1) were tested. The resultant Injected Charge versus Charge Centroid plot is shown in Figure 2-20. Error bars through representative points are shown.

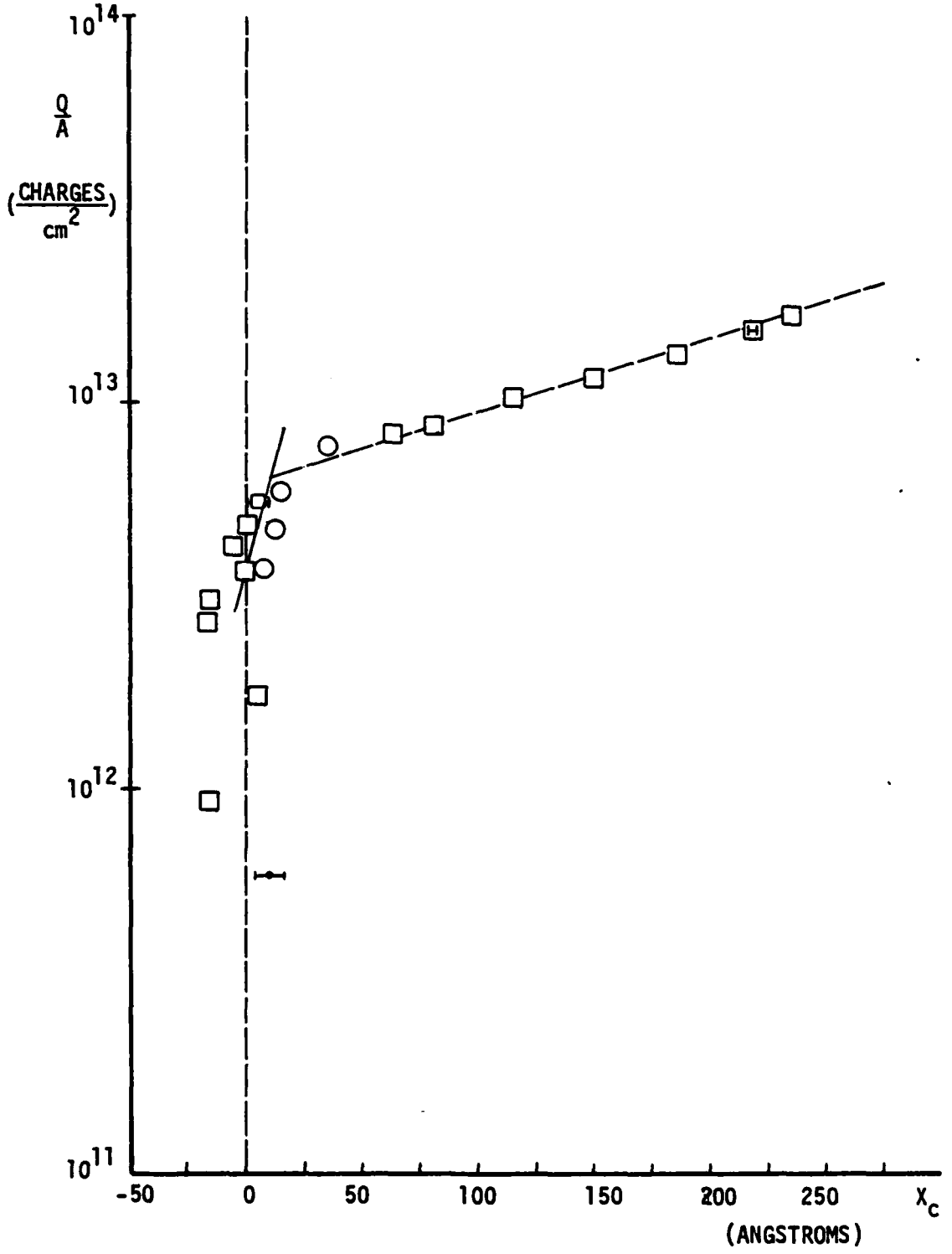


Figure 2-19: Injected Charge vs Centroid - Thin Oxide, High Dopant Density

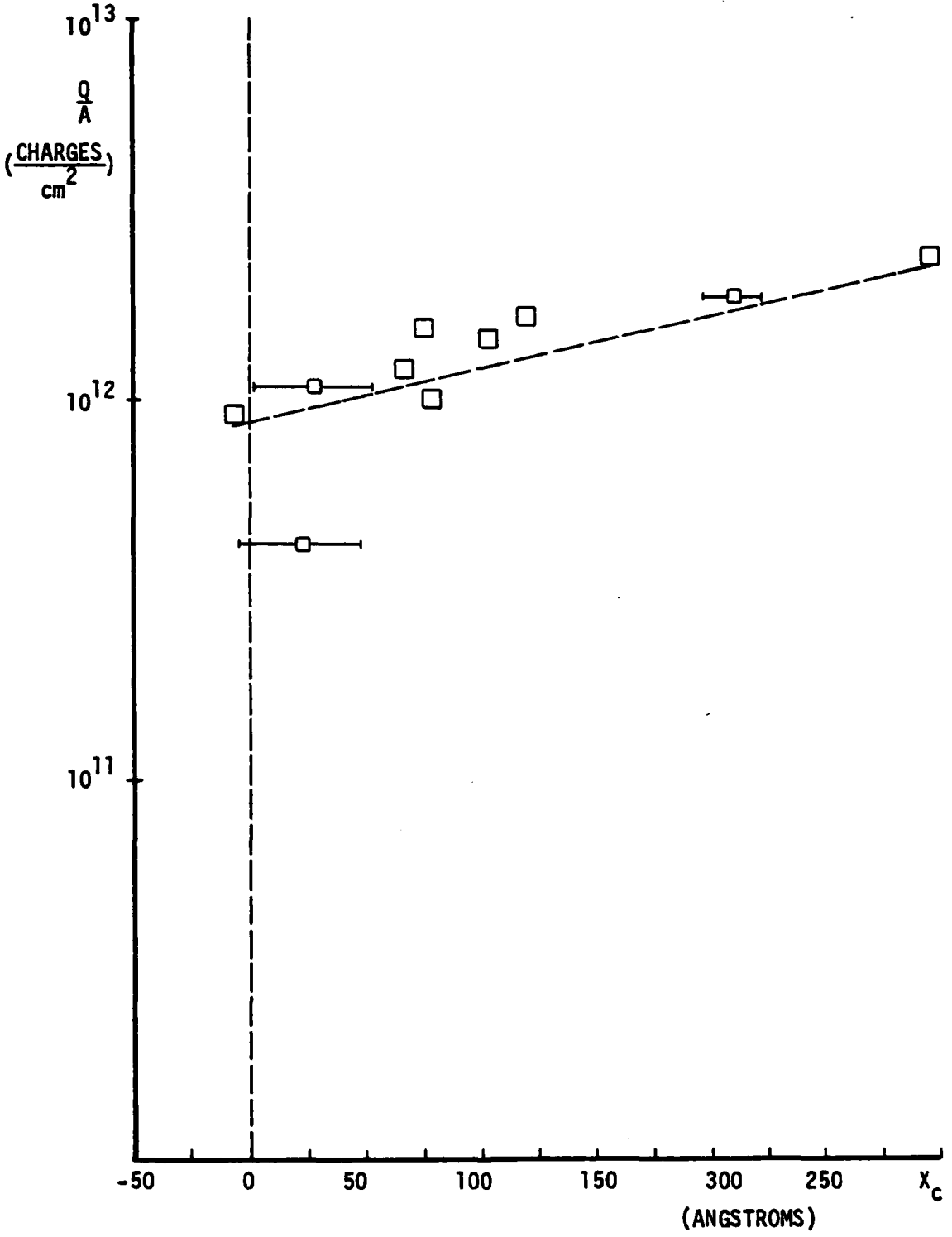


Figure 2-20: Injected Charge vs Centroid - Thick Oxide, Low Dopant Density

2.3.3 Observations

These experiments strikingly show the difference in location of trapped charges between interface doped devices and conventional MNOS devices. The conventional devices show the charge centroid to be at the mid-point of the nitride at the lowest measured values of charge injection. The interface doped devices exhibit localized charge trapping at the oxide-nitride interface up to a trap "saturation" level and then the charge centroid penetrates rapidly into the bulk nitride for additional injected charge. As the injected charge level increases, the centroid approaches the nitride mid-point value observed for devices with no interface dopant. This would indicate that the bulk nitride trap density is sufficiently large as to render the charges trapped at the oxide-nitride interface neglegible under high total charge injection conditions. The saturation level of injected charge in these experiments depended more on the oxide thickness than on the dopant density. The level of injected charge at which penetration into the bulk nitride which is apparent in Figure 2-19 for the thin oxide, high dopant density device (5 to 6 x 10^{12} cm^{-2}) is similar to that of the thin oxide, low dopant density devices which showed penetration when injected charge reached the 3 to 6 x 10^{12} cm^{-2} level as seen in Figure 2-18. The thick oxide devices having low dopant density displayed saturation at a much lower level (0.9 to 1.0 x 10^{12} cm^{-2} as shown in Figure 2-20) than the thin oxide devices of either low or high dopant density. A possible cause for this arises from the fact that for similar nitride thicknesses, applied gate voltages and stored charges, the thin oxide device will have a higher oxide electric field than the thick oxide device. This leads to a higher oxide current and consequent

high trapping rate, producing a rapid increase in stored charge. The thick oxide device, with a lower oxide current and thereby lower trapping rate, would require a longer charging period to achieve a comparable increase in stored charge level. During this longer period, detrapping and redistribution of charges further into the bulk nitride takes place causing the centroid to penetrate into the nitride. If a higher voltage on the thick oxide device is considered, to keep the charging period as short as for the thin oxide device, the resulting higher nitride electric field increases the Poole-Frenkle detrapping thus enhancing redistribution of charges further into the bulk nitride and hence increasing the centroid as compared to the thin oxide case. Additionally, as has been shown by others [73, 74, 75], the physical oxide-silicon interface does not exhibit a sharp transition but displays a gradual change from silicon to silicon oxide over a distance of 8 to 25 angstroms, depending primarily on the oxide thickness. This transition region would have a larger percentage effect on the energy barrier of the thin (30 angstroms) oxides than on the thick (85 angstroms) oxides. The effect being a lowering of the effective oxide barrier from the ideal 3.1 eV silicon-silicon oxide energy barrier. The physical thinness of the thin oxide would prevent the formation of the full 8 eV silicon dioxide energy band gap structure. Hence there would be an even greater oxide current, for the same oxide electric field, for this non-ideal structure than for the ideal thin oxide or the thick oxide structures.

3. CHAPTER THREE - THERMALLY STIMULATED CURRENTS

In this investigation the thermally stimulated current (TSC) technique was applied to various MIS structures under appreciable electric field conditions. The application of this electric field modifies the normal TSC because of the Poole-Frenkel effect: field assisted, thermal excitation. Specifically how this is handled is discussed in Sections 3.1.2 and 3.3.1.

3.1 Theory

3.1.1 Thermally Stimulated Current

The thermally stimulated release of trapped charges is often used to investigate the parameters of the trapping sites. When the carriers undergo non-radiative recombination the phenomenon measured is the thermally stimulated current or conductivity (TSC). Materials exhibiting radiative recombination of released charges can be investigated through thermally stimulated luminescence, traditionally called "glow curves". Both techniques provide a measure of the number of detrapped charges as a function of temperature and therefore are amenable to similar analysis procedures. Several different analytical approaches have been proposed in the literature.

Randall and Wilkins'[76] analysis was used as a basis by Grossweiner[77] who obtained an expression for trap depth below the conduction band of the form:

$$E_t = 1.51\ kT_m T_h/(T_m - T_h) \qquad (3.1)$$

where T_m = temperature of TSC curve peak maximum

T_h = temperature on low temperature side of TSC curve at the half maximum value

This expression assumes that the ratio of T_h to T_m is greater than 0.8 and that the ratio of trap attempt-to-escape frequency, ν, to heating rate, α, is greater than 10^7. The temperature ratio restriction is easily satisfied if the TSC peaks are narrow (distinct trap energy levels). The attempt-to-escape frequency is defined as:

$$\nu \equiv \sigma v_{th} N_c \tag{3.2}$$

where σ = trap capture cross section for carriers

v_{th} = carrier thermal velocity = $\sqrt{\frac{3kT}{m}}$

N_c = effective density of states in conduction band = $2h^{-3} (2\pi mkT)^{3/2}$

Hence, for a typical thermal velocity of 10^7 cm/sec, a capture cross section of 10^{-14} cm^2 would only require a conduction band density of states of 10^{14} cm^{-3} in order to satisfy the attempt-to-escape frequency assumption for a heating rate of one degree/second or slower. It should be noted that when calculating trap depths using equation (3.1) there is a term in the denominator which is the difference between two large numbers (T_m and T_h are both greater than 100 K) which are similar in value. This can lead to errors from a number of causes. (1) Several close peaks, merging to appear as a single peak, would exhibit an erroneously large $T_m - T_h$ value leading to an apparently small value for

a single trap depth. (2) An incorrect assumed value for the peak maximum intensity, due to not knowing the true value of the background or noise under the peak, would lead to an erroneous half maximum value and hence an inaccurate half maximum temperature.

Garlick and Gibson[78] proposed a method based on an analysis of the slope of the TSC curve on the low temperature side of the peak. Their expression for the intensity of the TSC curve was of the form:

$$I = I_o \exp[-E_t/kT - f(E_t,T)] \tag{3.3}$$

For low temperature the function $f(E_t,T)$ approached zero and therefore the slope of Ln I versus T^{-1} is equal to $-E_t/k$. Hoogenstraaten[79] points out that the drawback of this technique comes from having to use a "tail" of the TSC curve where any noise, background current or adjacent peaks may mask the actual TSC values. Figures 6 and 7 from his paper demonstrate that the portion of the TSC curve that must be used for the Ln I versus T^{-1} slope is actually below the 0.1 I_{max} level.

Haering and Adams[80] also used the work of Randall and Wilkins[76] as a basis, but they developed an expression for conductivity at the TSC curve maximum of the form:

$$\sigma(T_m) = \sigma_o \exp[-E_t/kT_m - 1] \tag{3.4}$$

where σ_o depends on material parameters and the number of charges in traps at $T \ll T_m$

In their development they note that the location of the TSC peak, T_m, varies with the heating rate. By assuming identical starting trap occupancy conditions for two TSC measurements at two different heating rates they consider σ_o to be constant and therefore eliminate it from the ratio $\sigma(T_{m1})/\sigma(T_{m2})$ using equation (3.4). As a result an expression for trap energy depth below the conduction band is obtained:

$$E_t = \frac{kT_{m1}T_{m2}\mathrm{Ln}(I_1/I_2)}{T_{m1} - T_{m2}} \tag{3.5}$$

where I_1 and I_2 are the maximums of the TSC peaks, located at T_{m1} and T_{m2} respectively, resulting from the measurements at the two different heating rates:

In general $T_{m1} - T_{m2}$ is small (10 to 15 degrees) compared to T_{m1} or T_{m2} (both > 100 K). This makes equation (3.5) very sensitive to accurate determination of the location of the TSC peaks. The presence of a broad peak makes determination of T_m subject to interpretation, introducing the possibility of large error into the calculation of the trap energy.

Bube[81, 82] developed an expression for the trap depth as a function of the temperature of the TSC peak maximum and the linear heating rate.

$$E_t = kT_m \,\mathrm{Ln}(N_c v_{th}\, \sigma k T^2/\alpha E_t) \tag{3.6}$$

where α = linear heating rate (degrees/second)

Substituting the expressions for thermal velocity and effective density

of states, a final expression relating trap energy, heating rate, and temperature at a TSC peak was formed:

$$E_t = kT_m \, Ln[(4\pi)^{3/2}\sqrt{\frac{3}{2}}(k/h)^3 m^* \sigma T_m^4/\alpha E_t] \tag{3.7}$$

3.1.2 Poole-Frenkel Barrier Lowering

The lowering of a bulk trap barrier upon application of an electric field is termed the Poole-Frenkel effect and is shown schematically in Figure 3-1. For a coulombic trap potential, electrostatic analysis leads to an expression for the potential barrier lowering:

$$\Delta\phi = \left(\frac{q}{\pi\varepsilon}\right)^{1/2} F^{1/2} \equiv \beta F^{1/2} \tag{3.8}$$

ε = permittivity of the material
F = electric field
β = Poole-Frenkel constant

Under applied electric field conditions calculations based simply on thermal excitation emission peaks (such as described in Section 3.1.1) will result in the value $E_t - \Delta\phi$. Hence the energy difference due to the Poole-Frenkel effect must be added to obtain the true zero-field trap depth.

Conduction in silicon nitride is by the Poole-Frenkel effect [23, 83, 84] and is of the general form:

$$J = J_o \exp\,[-(q/kT)(E_t - \beta F^{1/2})] \tag{3.9}$$

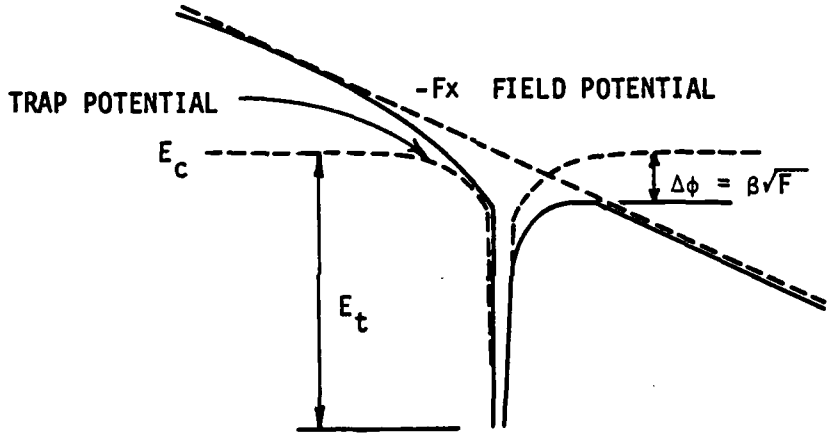


Figure 3-1: Trap Barrier Lowering by Applied Field: Poole-Frenkel Effect

A plot of the log of the current versus square root of applied field yields the Poole-Frenkel constant.

3.2 Experimental Equipment and Data Acquisition Procedures

3.2.1 Thermally Stimulated Current System

The TSC system used is shown in Figure 3-2. The temperature/rate controller was capable of producing a range of heating rates from 0.7 to 3.6 degrees per second over a temperature span of 73 K to 600 K. Measurement over a range of $-200^{o}C$ to $200^{o}C$ showed a temperature-time linearity to within less than $0.8^{o}C$. While controlling the temperature of the sample mounted on the "cold finger" through the thermocouple/heater-current loop, the temperature/rate controller produced an output proportional to the device temperature for the X-axis of the X-Y recorder.

The bias supply was used to force thermally detrapped electrons from the nitride, the interface dopant, the oxide-nitride interface and the silicon-silicon oxide interface to pass through the silicon substrate or through the nitride to the picoammeter. Dry cells were used to reduce ground loop currents. Available electronic power supplies introduced irreducible ground loop currents greater thann 400 picoamps with no sample connected to the leads at the "cold finger". The dry cell approach resulted in measured "currents" with no sample connected to the leads at the "cold finger" on the order of 0.2 to 1 picoamp. The output of the picoammeter (model HP 610B) was applied to the Y-axis of the X-Y recorder to record the thermally stimulated

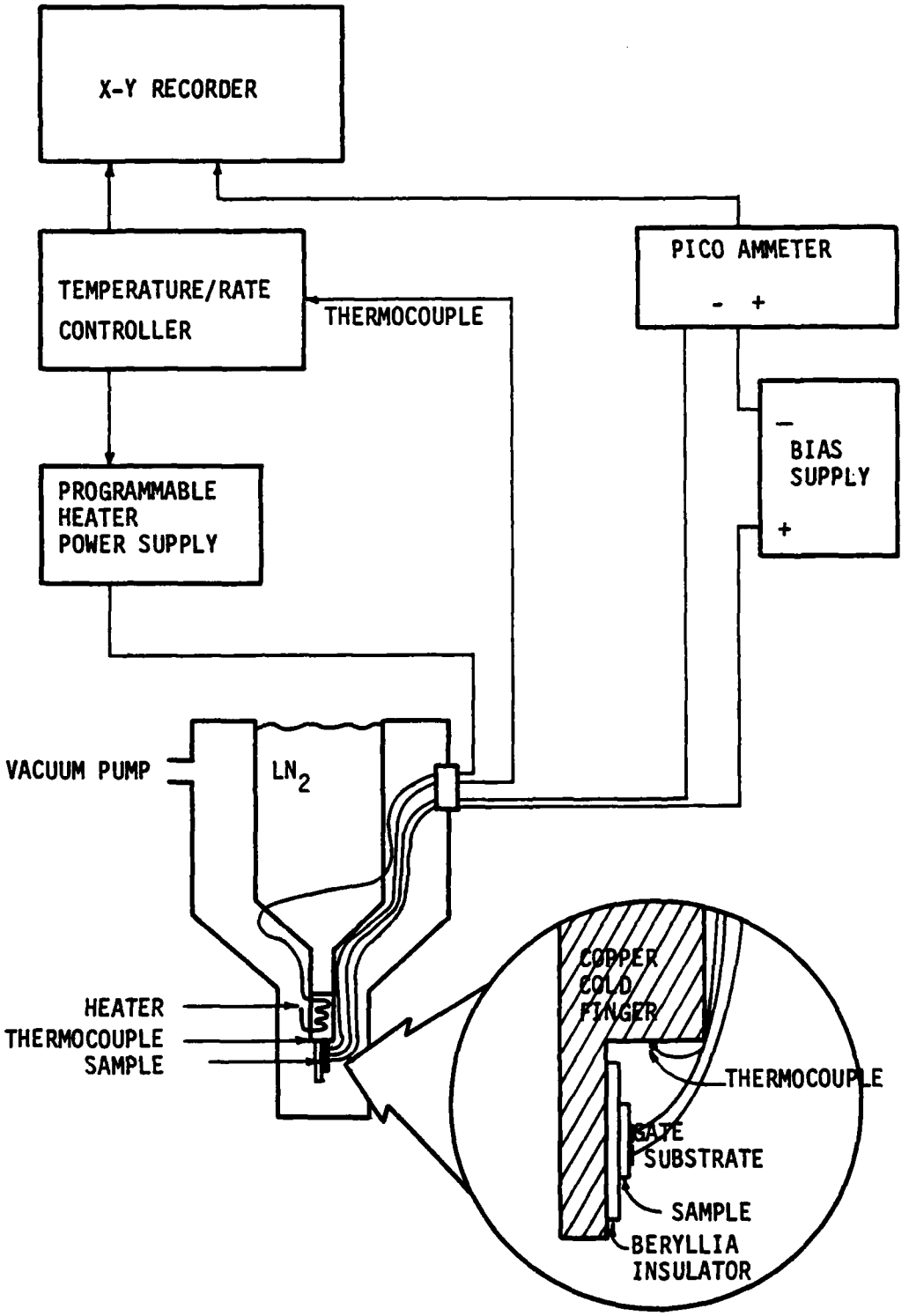


Figure 3-2: Thermally Stimulated Current System

current.

Low noise coax cables were used for the heater power and all signal runs within the dewar. Triax cables were used between the dewar and the bias supply and the picoammeter. A short section of coax was used between the bias supply and the picoammeter. The TSC and temperature/time output signals were in the 0 to 10 volt range.

3.2.2 Data Acquisition Procedures

Each TSC measurement was accomplished as follows:

- The initial charge condition of a device was established by positive or negative write pulses and characterized at room temperature by determination of the zero voltage capacitance and the flatband capacitance voltage. When electron traps in the device were filled the flatband voltage was several volts negative and the zero voltage capacitance showed values corresponding to silicon surface accumulation conditions.
- The device was cooled to liquid nitrogen temperature under a bias, V_c. Normally $V_c = 0$.
- The TSC bias was applied and the temperature/rate controller was activated to raise the temperature from $-190^{o}C$ to $300^{o}C$ at 0.1, 0.25 or 0.5 degrees per second. The thermally stimulated current versus time/temperature was recorded on the X-Y recorder.
- At $300^{o}C$ the TSC signal was disconnected and the device cooled to room temperature under the same TSC bias.
- At room temperature the zero voltage capacitance and flatband capacitance voltage were again determined to verify the stored charge loss from the device.

Typical TSC curves showing electron discharge from filled traps and lack of electron discharge due to previously emptying the traps are shown in Figure 3-3.

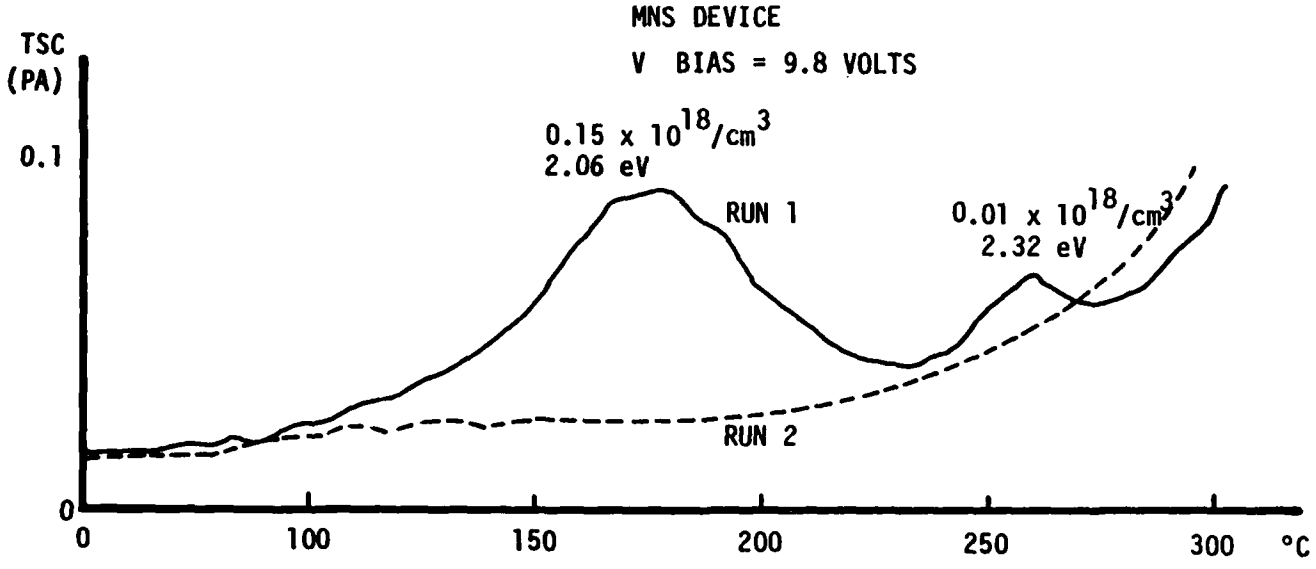


Figure 3-3: TSC Curves from a Device with Filled Traps and After Trap Discharge

3.3 Data Analysis Procedures

3.3.1 Trap Energy Level Determination

TSC Analysis Techniques

For this effort an analysis technique for calculating the trap depths had to be selected. After data acquisition, as described above, was accomplished on two devices (a total of ten TSC measurements) the trap depths for the TSC peaks were calculated using the three techniques described in Section 3.1.1, using equations (3.1), (3.5) and (3.7) (Grossweiner (G), Haering and Adams (H&A) and Bube (B) respectively). The measured data (heating rate, half max temperature, temperature at peak maximum, current at peak maximum) and the calculated trap energies are shown in Table 3-1. The multiple trap depths or lack of an energy level entry for certain runs reflect the need to use data from two measurements having differing heating rates in the technique developed by Haering and Adams (equation (3.5)).

Of the three methods of TSC analysis it was noted that Bube's method was the most consistent. The temperature of the maximum of the peaks is extracted from the TSC curves, and heating rate is included explicitly. Grossweiner's method produced a wider trap depth spread for a given TSC peak for variations in heating rate. It produced a shallower trap depth when T_m was less than 0^oC and a deeper trap depth when T_m was much above 0^o (as compared to Bube's). Grossweiner's method requires that the temperature of the maximum of the peaks plus the temperature of the half maximum of the peaks be extracted from the TSC

Device/ Run		α (%S)	T_h (°C)	T_m (°C)	I_m (pA)	E (eV) H&A	E (eV) G	E (eV) B
A	1	.5	-142	-132	18.2		.24	.42
	2	.25	-145	-135	7.3	.51	.23	.41
	3	.25	-148	-135	7.7	.48	.17	.41
	4	.1	-150	-137	2.9	.73	.17	.42
						1.05		
						1.09		
	5	.1	-150	-140	2.9	.61	.17	.41
						.76		
						.80		
A	1	.5	-20	- 5	52.2		.59	.83
	2	.25	-30	-17	27.2	.32	.62	.81
	3	.25	-25	-10	30.5	.65	.57	.83
	4	.1	-44	-32	14.8	.26	.60	.78
						.22		
						.18		
	5	.1	-37	-27	18.5	.27	.76	.79
						.21		
						.16		
A	1	.5	8	17	12.0		1.18	.91
	2	.25	- 3	5	22.0	-.35	1.22	.88
	3	.25	0	10	15.5	-.26	1.01	.90
	4	.1	-20	-10	14.0	-.04	.87	.85
						.19		
						.03		
	5	.1	-17	- 5	14.0	-.05	.75	.87
						.29		
						.04		
B	1	.5	-52	-35	64.3		.40	.73
	2	.5	-62	-45	69.5		.37	.70
	3	.5	-62	-45	69.5		.37	.70
	4	.25	-75	-63	73.0	-.02	.45	.65
						-.01		
						-.01		
	5	.25	-77	-64	70.0	-.01	.41	.65
						-.002		
						-.002		
B	1	.5	20	27	2.5		1.64	.94
	2	.5	15	23	2.7		1.39	.93
	3	.5	20	34	13.5		.83	.97
	4	.25	3	17	5.3	-.56	.75	.92
						-.83		
						.42		

Table 3-1: Calculated Trap Depths (Haering and Adams, Grossweiner and Bube Analyses)

curves. The heating rate is included implicitly through the maximum/half maximum ratio. The shallower calculated depth can be attributed to the existence of a number of closely spaced trap levels (or a band of trap energies) rather than a single distinct level. The deeper calculated trap depths at high T_m can be explained by an improperly selected half max temperature. An increased background current at high temperatures would mask part of the peak and assumption of too high a background current while determining the half max value and half max temperature would cause this temperature to be chosen too close to the temperature of the peak maximum. This would cause a larger calculated trap energy. Haering and Adams' method yielded a wide spread of trap energy levels. This is attributed to the fact that not all initial conditions of these runs were identical, although this is required in order to use the Haering and Adams development. The measured currents for the various heating rate runs do not arise from identical initial charge storage conditions and thus invalidate this analysis technique for this investigation.

All subsequent trap depth calculations from TSC peak data were performed using Bube's technique (equation (3.7)).

Following TSC measurements on MNS, standard MNOS and interface doped MNOS capacitor structures, trap depths were calculated (equation (3.7)) for all identifiable peaks. When two peaks were sufficiently close as to overlap, they were decomposed into a major and a minor peak. The minor peak was reconstructed by assuming a shape for the major peak and subtracting this from the composite curve. This insured that the maximum of the minor peak could be correctly located for determination

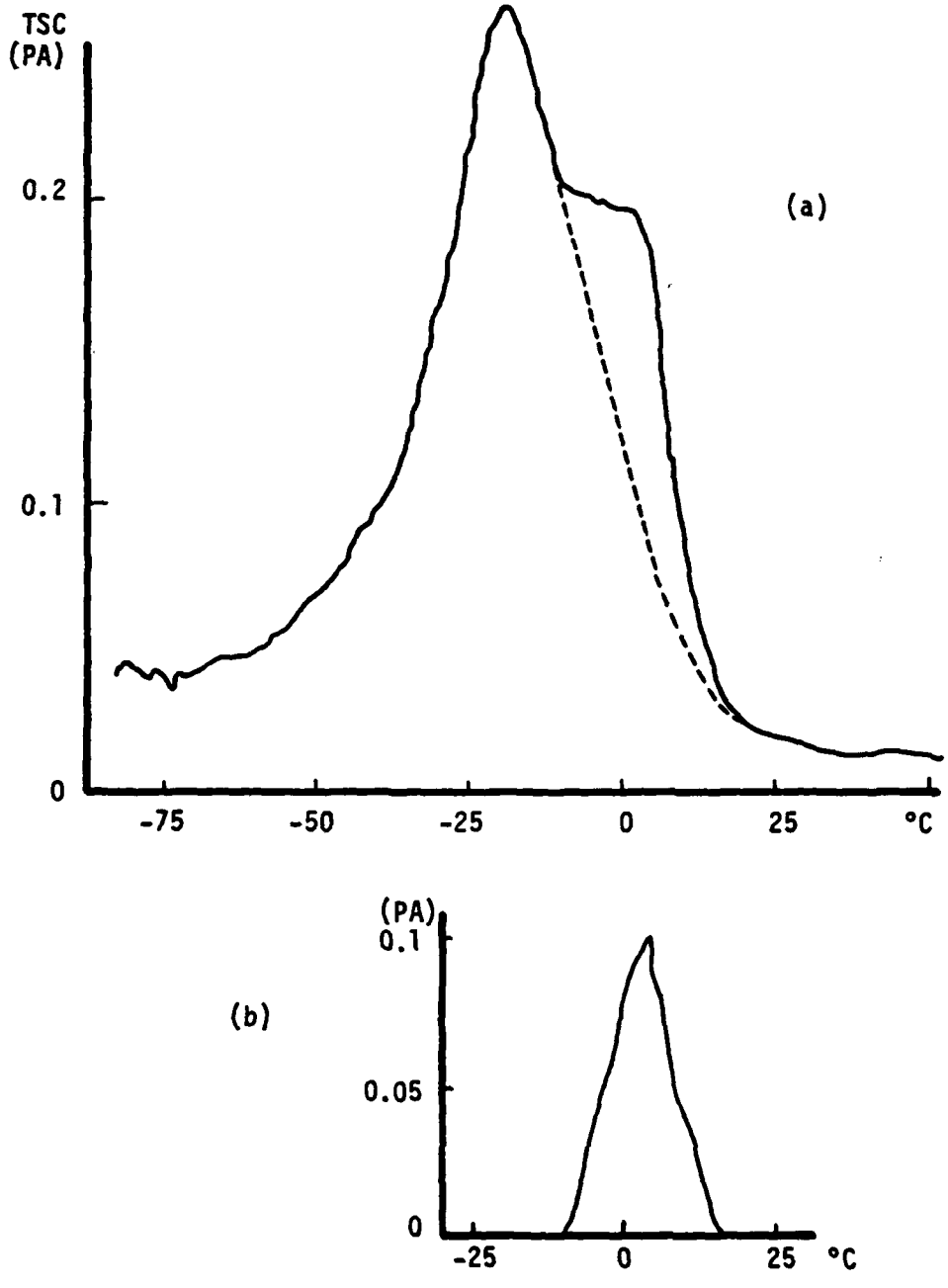


Figure 3-4: Decomposition of Overlapping Peaks

of T_m. An example of this is shown in Figure 3-4. It was then assumed that:

1. MNS structures could produce bulk nitride trap levels and silicon-silicon nitride interface trap levels.
2. Standard MNOS structures could produce bulk nitride trap levels, oxide-nitride interface trap levels and silicon-silicon oxide interface trap levels.
3. Interface doped MNOS structures could produce bulk nitride trap levels, oxide-nitride interface trap levels, silicon-silicon oxide interface trap levels and interface dopant induced trap levels.

By assuming the existance of only these possible trap levels and by controlling the material parameters of the devices through common starting material and subsequent fabrication materials and processes, a comparison of the trap "spectra" of the different types of device structures yielded energy bands which could then be paired with each of the trap types described above.

Silicon-Insulator Interface States Analysis

The trap depths calculated from the TSC data, using equation (3.7), in the range 0 to 1.1 eV were plotted to check for the existence of silicon-silicon oxide interface states effects. No Poole-Frenkel effect corrections were necessary for this plot. Only the range 0.3 to 0.5 eV exhibited TSC peaks exclusively for structures with silicon-silicon oxide interfaces (Types B - E, Table 3-2) while excluding TSC peaks from positive gate bias conditions. (After thermal excitation at the silicon-silicon oxide interface only a negative gate bias could cause the emitted charges to create a measurable current flow. The silicon

oxide barrier would block charge flow under positive gate bias conditions.) The same energy region was examined for effects of silicon-silicon nitride interface traps. The data did not show unequivocal evidence of silicon-silicon nitride interface traps. Hence this type of trap was not considered in the remainder of the analysis.

Inclusion of Poole-Frenkel Barrier Lowering

The Poole-Frenkel barrier lowering was then calculated for each of the remaining data points based on the magnitude and polarity of the nitride electric field in each structure at the temperature of the TSC peaks. These barrier lowering values were added to the energy depths calculated from equation (3.7) for the data points.

The traps in the MNS structure (now assumed to have only bulk nitride traps), being distributed throughout the nitride layer, exhibit Poole-Frenkel barrier lowering under both positive and negative bias. Hence the MNS structure Poole-Frenkel corrected trap depths defined the final nitride trap ranges, which were then plotted.

The Poole-Frenkel corrected trap depths from standard and interface doped MNOS structures were then plotted. Any of these data points which fell into a previously defined nitride trap range were considered to be bulk nitride trap effects caused by the MNOS nitride layer.

The remaining data points were considered to be caused by dopant induced traps or oxide-nitride interface traps. Both types of traps are spatially located at the oxide-nitride interface. Therefore the

Poole-Frenkel barrier lowering is appropriate only for positive gate bias conditions. A positive gate bias induces a field assisted, thermal excitation of charges from the oxide-nitride interface region into the nitride conduction band and subsequent nitride conduction. A negative gate bias creates a current flow through the oxide from electrons emitted from the oxide-nitride interface region. The silicon oxide conduction mechanism under the field conditions existing during the TSC experiments is Fowler-Nordheim tunneling from the nitride conduction band into the oxide conduction band.[71, 85] Hence, under the negative bias conditions, there is no Poole-Frenkel barrier lowering and the uncorrected trap depth as calculated by equation (3.7) is the true value. In order to reflect this, the Poole-Frenkel barrier lowering factor was subtracted from the dopant induced trap and oxide-nitride interface trap data points which resulted from runs with negative gate bias. The resultant data points were replotted and the devices' trap spectra comparison was completed and the trap type associated with each energy range segment was determined.

3.3.2 Trap Spatial Density Analysis Technique

The charge centroid experiments provided information on the total number of charges trapped in the entire MNOS structure. The TSC measurements provide information on the number of charges which can be trapped in each type of trap in the structure under investigation.

Each peak identified for trap energy depth analysis was used for a calculation of number of charges released. The number of released charges, N_t, is the integral of the thermally stimulated current over the time duration of the TSC peak.

$$N_t = \int_{t_1}^{t_2} \frac{I}{q}\, dt$$

However, $T = T_o + \alpha\, t$ for a linear heating rate.

Therefore:

$$N_t = \int_{T_1}^{T_2} \frac{I}{\alpha q}\, dT$$

A triangular area approximation to this integral was used to calculate the charge density (number of charges per square centimeter for interface traps and number of charges per cubic centimeter for bulk nitride traps) represented by each peak or decomposed peak. Figure 3-5 shows the data extracted from each peak for use in equation (3.10) for calculating trap density.

$$N_t = \frac{1}{2}\,[(T_3-T_2)I_1+(T_2-T_1)I_3+(T_1-T_3)I_2]/(\alpha\, q\, A) \qquad (3.10)$$

where α = heating rate (degrees/second)

A = area of device (cm^2)

I_i = thermally stimulated current at point i (amps)

T_i = temperature at point i (degrees C)

N_t = number of charges per square centimeter

Normally T_i and I_i, i=1,3 were all different. However, as can be seen in Figure 3-5(b), when overlapping peaks were decomposed I_1 and I_2 for the minor peak were, by definition, both identically zero.

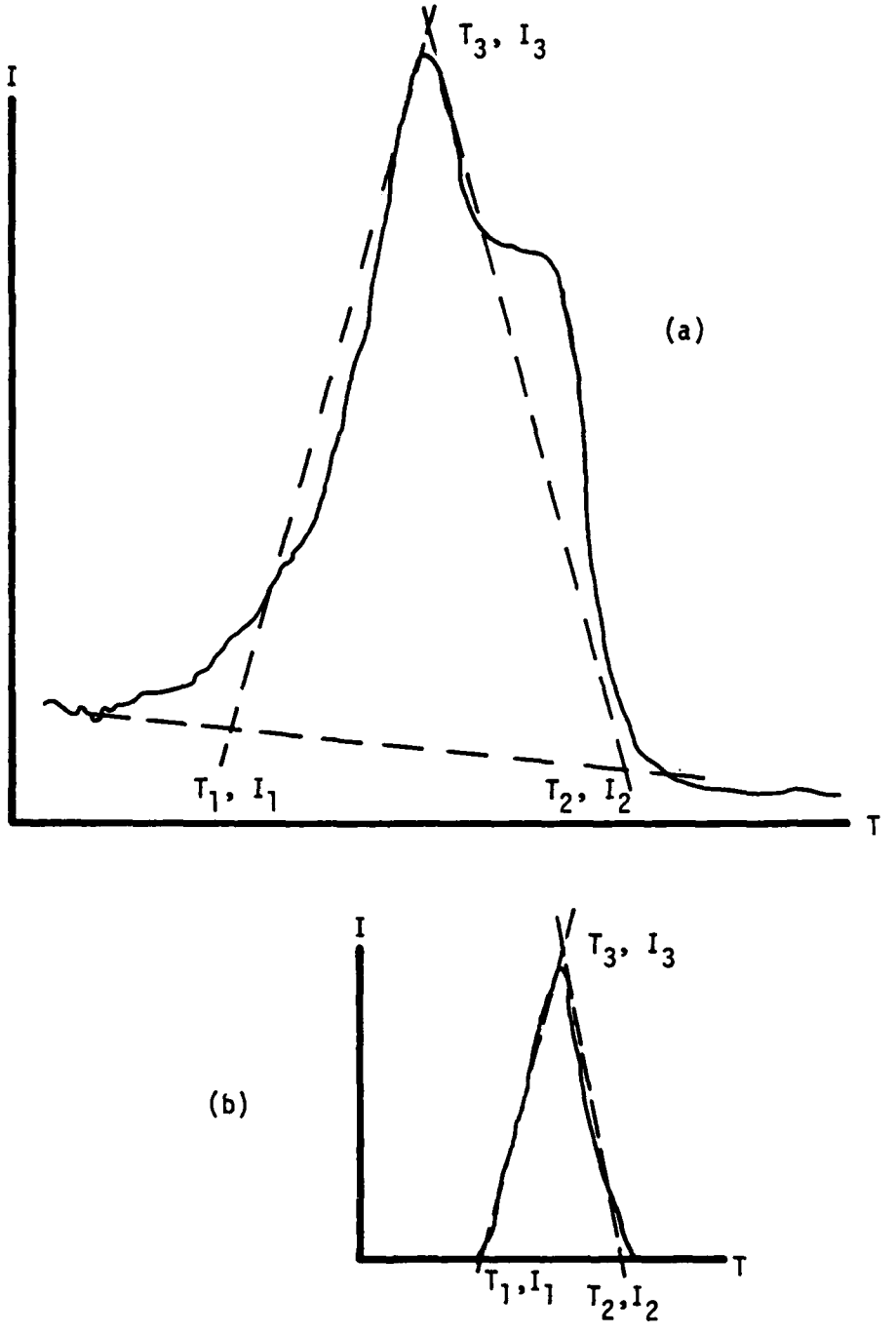


Figure 3-5: Trap Density Calculation Parameters

Bulk nitride trap volume density was obtained by dividing N_t by the device nitride thickness.

3.4 Results

The devices used for TSC measurements were MIS capacitor structures with 50 mil diameter contacts (0.012 cm^2 area) fabricated on 5 ohm-cm, n-type, (100), silicon substrates with gold as the insulator and substrate contacts metalization. MNS, standard MNOS and interface doped MNOS structures were examined. The thin thermal oxide was grown at 900°C in a 20 percent dry oxygen atmosphere with a nitrogen carrier gas. The nitrides were deposited in a hot wall system by the thermal decomposition of dichlorosilane (SiH_2Cl_2) in the presence of ammonia (NH_4) at 770°C with nitrogen as the carrier gas. The NH_4:SiH_2Cl_2 ratio was 1000:1. The interface dopant, tungsten, was deposited using electron beam evaporation. Dopant density of these monolayer range tungsten films was controlled by a quartz crystal thickness monitor which had been calibrated by Rutherford Backscattering (RBS) analysis of the tungsten atomic concentrations in interface doped nitride-oxide-silicon structures[86] fabricated by the same process as those used for the TSC measurements. External contact to the MIS capacitor device gate and substrate metalization was by spring loaded needle point probes. The nitride and oxide thickness and tungsten dopant density parameters for the five types of devices measured are shown in Table 3-2.

	Nitride Thickness (angstroms)	Oxide Thickness (angstroms)	Tungsten Density (number/cm^2)
A	422	None	None
B	456	35	None
C	456	85	None
D	439	82	7×10^{15}
E	438	32	2×10^{15}

Table 3-2: Device Parameters

The data from five different MNS devices (Type A in Table 3-2) resulting from a total of 25 TSC runs was taken to obtain the spectrum of the MNS structure. The trap energy depths were calculated to be in the range 1.14 eV to 2.25 eV.

The data from four different thin oxide conventional MNOS devices (Type B in Table 3-2) resulting from a total of 16 TSC runs was taken to obtain the spectrum of one form of standard MNOS structure. The trap energy depths were calculated to be in the range 0.4 eV to 2.32 eV.

The data from six different thick oxide conventional MNOS devices (Type C in Table 3-2) resulting from a total of 31 TSC runs was taken to obtain the spectrum of a second form of standard MNOS structure. The trap energy depths were calculated to be in the range 0.3 eV to 2.23 eV.

The data from seven different thick oxide, high dopant density, interface doped MNOS devices (Type D in Table 3-2) resulting from a total of 26 TSC runs was taken to obtain the spectrum of an interface doped MNOS structure. The calculated trap energy depths ranged from

1.18 eV to 2.32 eV.

The data from three different thin oxide, low dopant density, interface doped MNOS devices (Type E in Table 3-2) resulting from six TSC runs was used to compare a thin oxide, intentionally doped device to the Type B, standard thin oxide device. Only a limited number of runs was completed due to premature "breakdown" of the insulating properties of the interface doped dual dielectric. Two effects were observed. (1) Many devices were too conductive, as fabricated, to show any TSC effects in the experimental system. (2) Those devices which did not display overly high, as fabricated, conductivity, did degrade after only two high temperature runs to unacceptably high conductivity conditions. These effects are attributed to dopant penetration into the oxide changing its conductivity charactistics. The limited TSC data yielded calculated trap energy depths ranging from 0.42 eV to 2.11 eV.

A summary of the energy levels and trap densities results to be discussed in this section is shown in Table 3-3, page 122.

Figures 3-6 through 3-8 show the spectra of the calculated energy depths versus device type. Each data point represents a TSC peak. Coincident trap depths are indicated by a numeral showing the number of independent peaks yielding that depth. The charge trapping location that was paired up with each energy range (discussed in Section 3.4.1) is indicated, and a calculated emission temperature for a zero electric field condition is also noted. Figure 3-6 shows the energy ranges of 0.3 to 0.5 eV below the <u>silicon</u> conduction band and 0.7 to 1.0 eV below the <u>silicon nitride</u> conduction band (silicon-silicon oxide surface

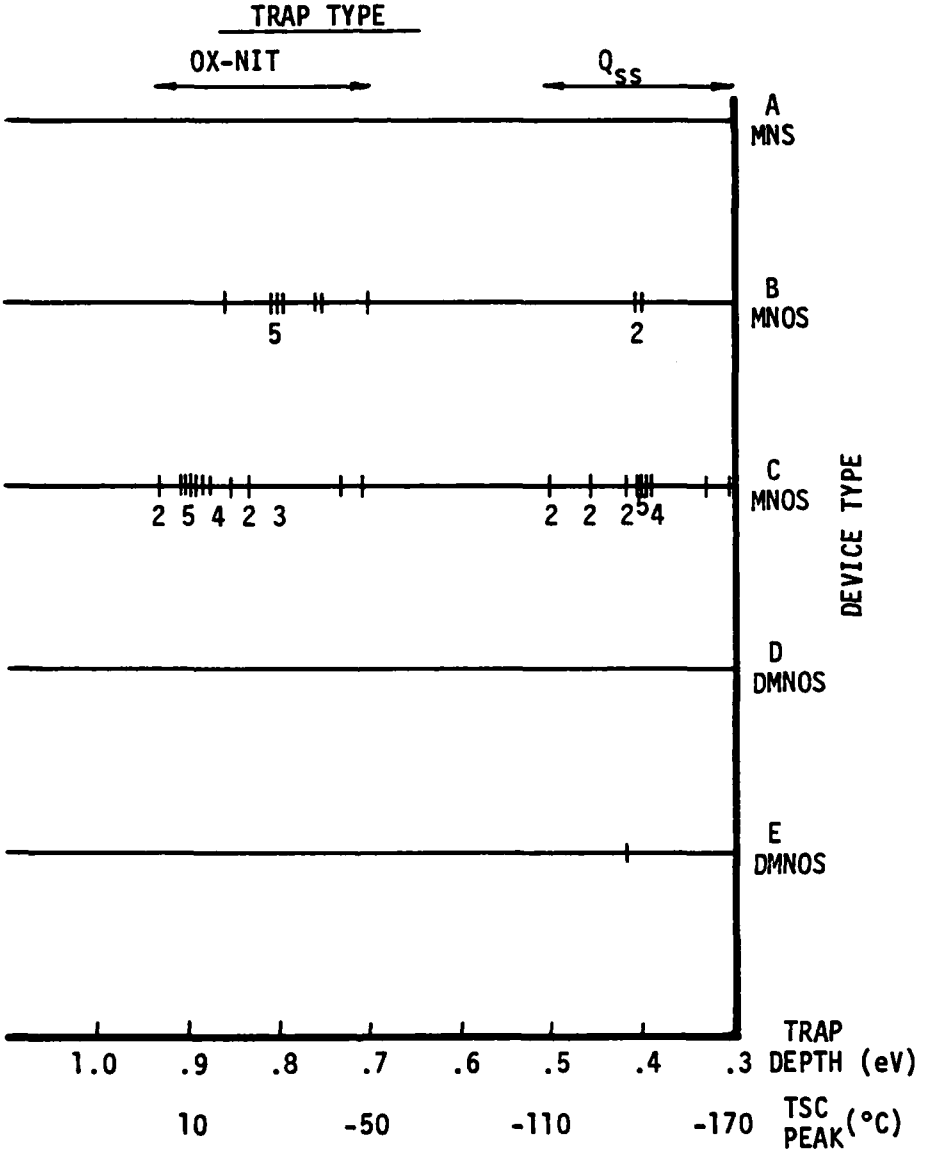


Figure 3-6: TSC Energy Spectrum vs Device Structure (Table 3-2) (0.3 to 0.5 and 0.7 to 1.0 eV) and Deduced Trap Site

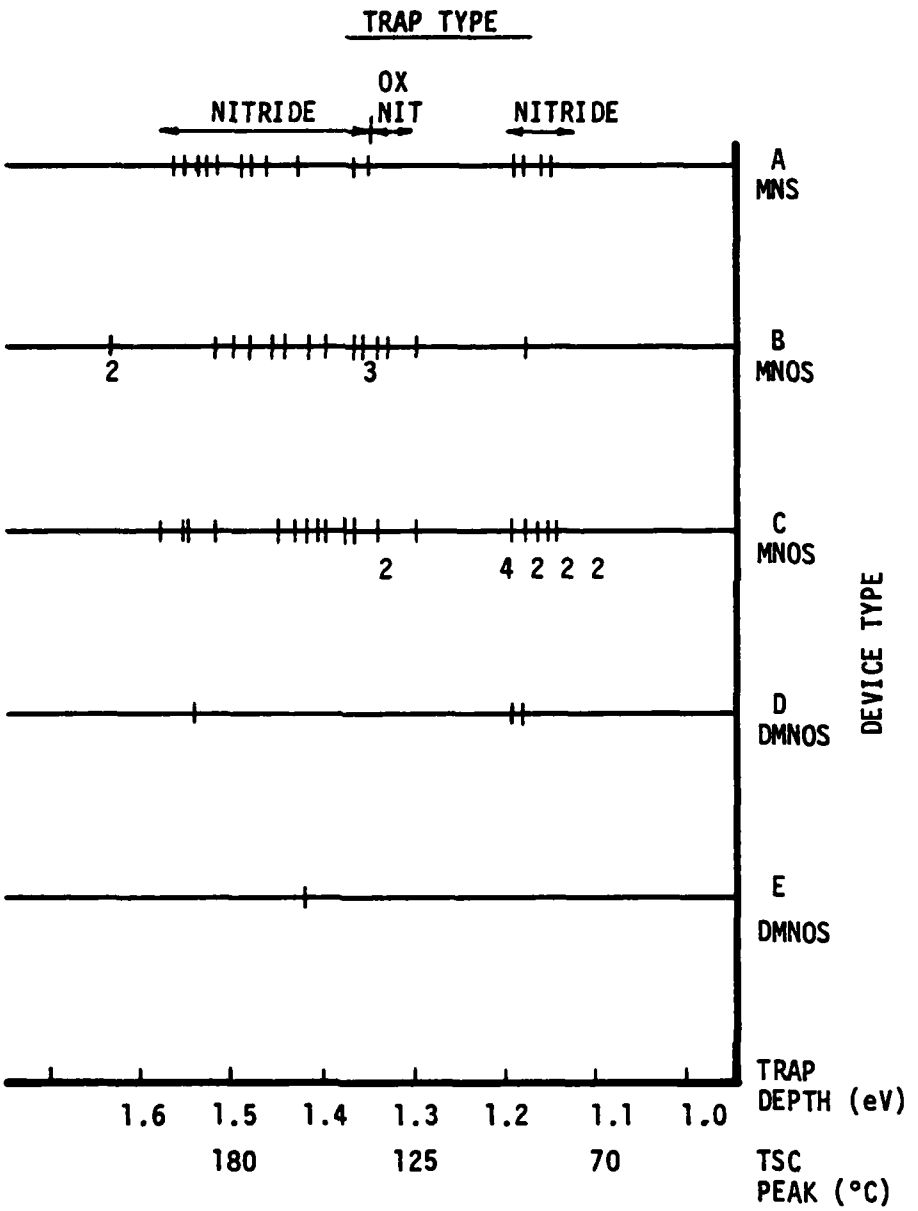


Figure 3-7: TSC Energy Spectrum vs Device Structure (Table 3-2) (1.0 to 1.65 eV) and Deduced Trap Site

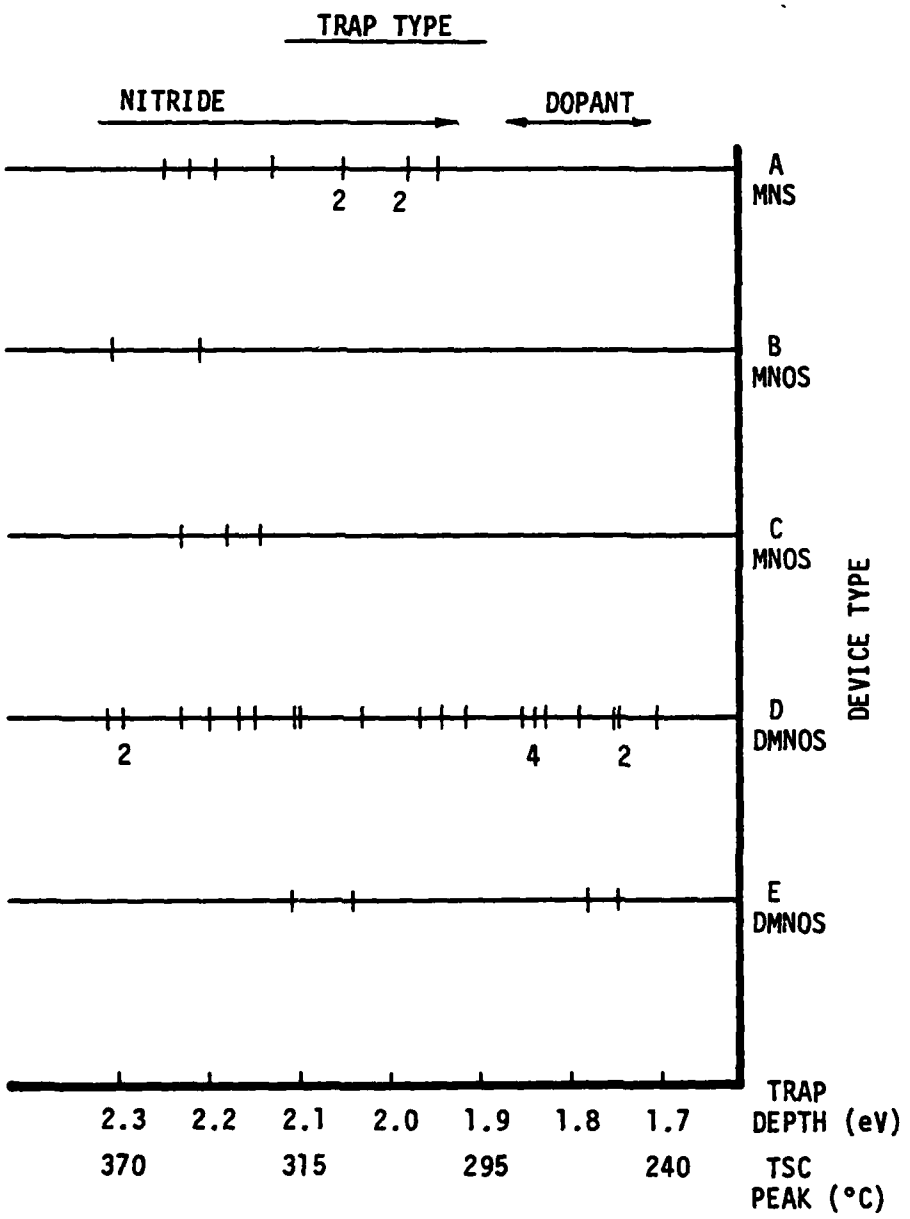


Figure 3-8: TSC Energy Spectrum vs Device Structure (Table 3-2) (1.65 to 2.32 eV) and Deduced Trap Site

states and shallow oxide-nitride interface traps). Figure 3-7 shows the energy range of 1.0 to 1.65 eV below the silicon nitride conduction band (bulk nitride traps and deep oxide-nitride interface traps). Figure 3-8 shows the energy range of 1.65 to 2.4 eV below the silicon nitride conduction band (dopant induced traps and deep bulk nitride traps).

3.4.1 Energy Level Assignment Results

The electron emission resulting in traps calculated to be 1.71 to 1.86 eV below the nitride conduction band was associated with the tungsten interface dopant. These levels were seen in the two types of interface doped MNOS structures but were not observed in the MNS or the standard MNOS structures. It should be noted that in spite of the very limited data from the thin oxide, low dopant density (Type E) device, data points within the interface dopant energy range were obtained.

Electron emission resulting in trap depths calculated as 1.92 to 2.32 eV below the nitride conduction band was observed for all types of structures and therefore was attributed to traps in the common layer, the bulk nitride traps. Yeargan and Taylor[83] have reported bulk nitride traps 2.0 and 2.25 eV below the nitride conduction band, while Jacobs and Dorda[87] have deduced trap levels between 1.92 and 2.77 eV below the nitride conduction band.

The electron emission peaks leading to trap depths calculated to be 1.35 to 1.58 eV below the nitride conduction band were seen predominantly in MNS and both types of standard MNOS structures. This is attributed to emission from medium depth traps in the bulk nitride. Traps in this energy range and in the deep bulk nitride range described

above have been proposed by Svensson[40] to describe conduction in silicon nitride. Lehovic and Fedotowski[46] have deduced a 1.5 eV trap level from retention measurements on MNOS devices. Additionally, they postulate (but do not calculate) shallower traps to explain deviations of experimental data from their single trap model calculations. The traps near 1.15 eV, described below, support their postulation.

The emission peaks resulting in calculated trap depths in the range 1.30 to 1.34 eV below the nitride conduction band are seen only with the standard MNOS structures and are attributed to deep oxide-nitride interface traps.

The emission peaks resulting in calculated trap depths in the range 1.14 to 1.19 eV below the nitride conduction band are exhibited by MNS, standard MNOS and interface doped MNOS structures and are assumed to be shallow bulk nitride traps from the common nitride layer in all three types of devices. Traps from this range through 2.4 eV were deduced from MNOS retention curves by Lundkvist et al.[42, 43]

Electron emission resulting in trap depths calculated as 0.70 to 0.93 eV below the nitride conduction band was seen only in the standard MNOS structure spectra and is therefore associated with shallow oxide-nitride interface traps.

Electron emission from silicon-silicon oxide surface states 0.3 to 0.5 eV below the silicon conduction band was observed. This emission was seen at low temperatures (-170°C to -110°C), only under negative gate bias and in standard and interface doped MNOS structures but not in MNS structures.

3.4.2 Trap Density Results

The analyses of trap spatial densities, as described in Section 3.3.2, generated spatial density versus trap energy level data. This data was plotted for each trap energy range identified in Section 3.4.1. Because the initial trap occupancy conditions for the many trap types and trap levels could not be independently controlled, different TSC runs produced different numbers of thermally excited electrons. However, plotting all the results provided bounds on the trap densities and some structure trends within the trap energy ranges.

Dopant Induced Trap Densities

Figure 3-9 shows the calculated trap densities (numbers of traps per square centimeter) for trapping levels associated with the tungsten interface dopant. Over the range 1.71 to 1.86 eV there appear to be two density peaks, $3 \times 10^{12} cms^{-2}$ and $5.5 \times 10^{12} cms^{-2}$, at 1.76 and 1.84 eV respectively.

Oxide-Nitride Interface Trap Densities

Figure 3-10 shows the calculated trap densities for both ranges of trapping levels associated with the oxide-nitride interface. The shallow traps (0.70 to 0.93 eV below the nitride conduction band) appear to have a symmetric, gradually peaking, trap density distribution with a maximum on the order of $5 \times 10^{12} cms^{-2}$ centered at 0.8 eV. The narrow range encompassing the deep oxide-nitride interface traps exhibited trap densities up to $30 \times 10^{12} cms^{-2}$.

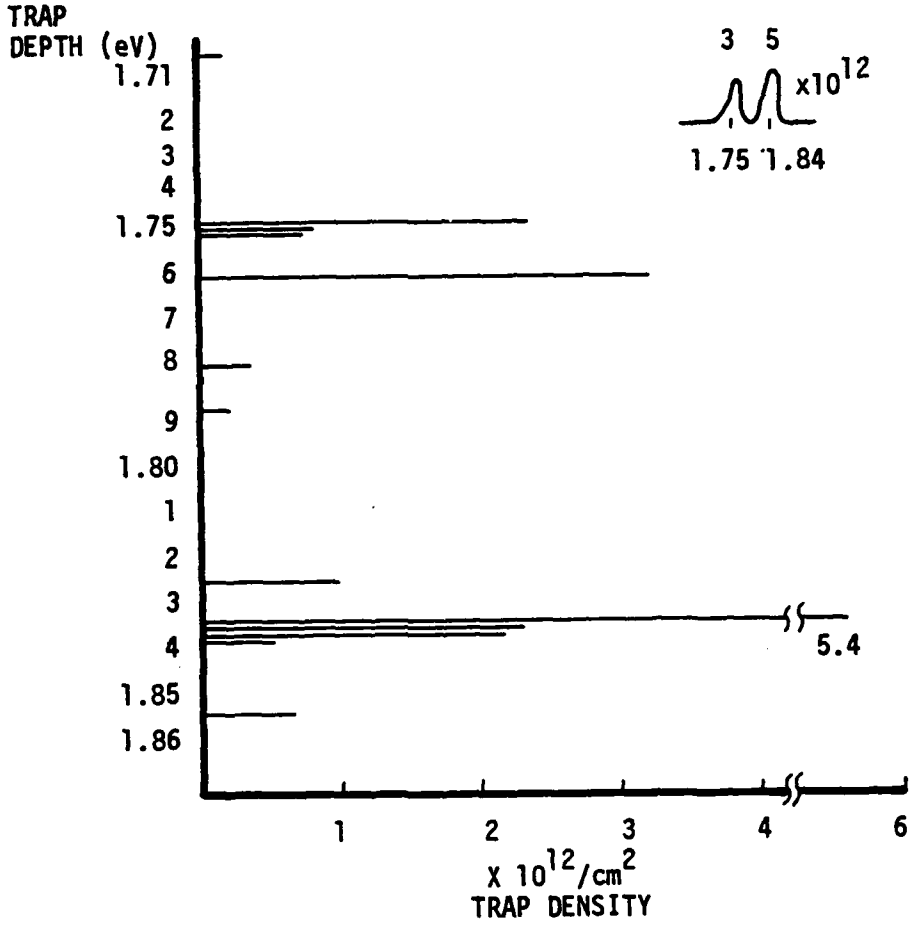


Figure 3-9: Tungsten Interface Dopant Trap Densities

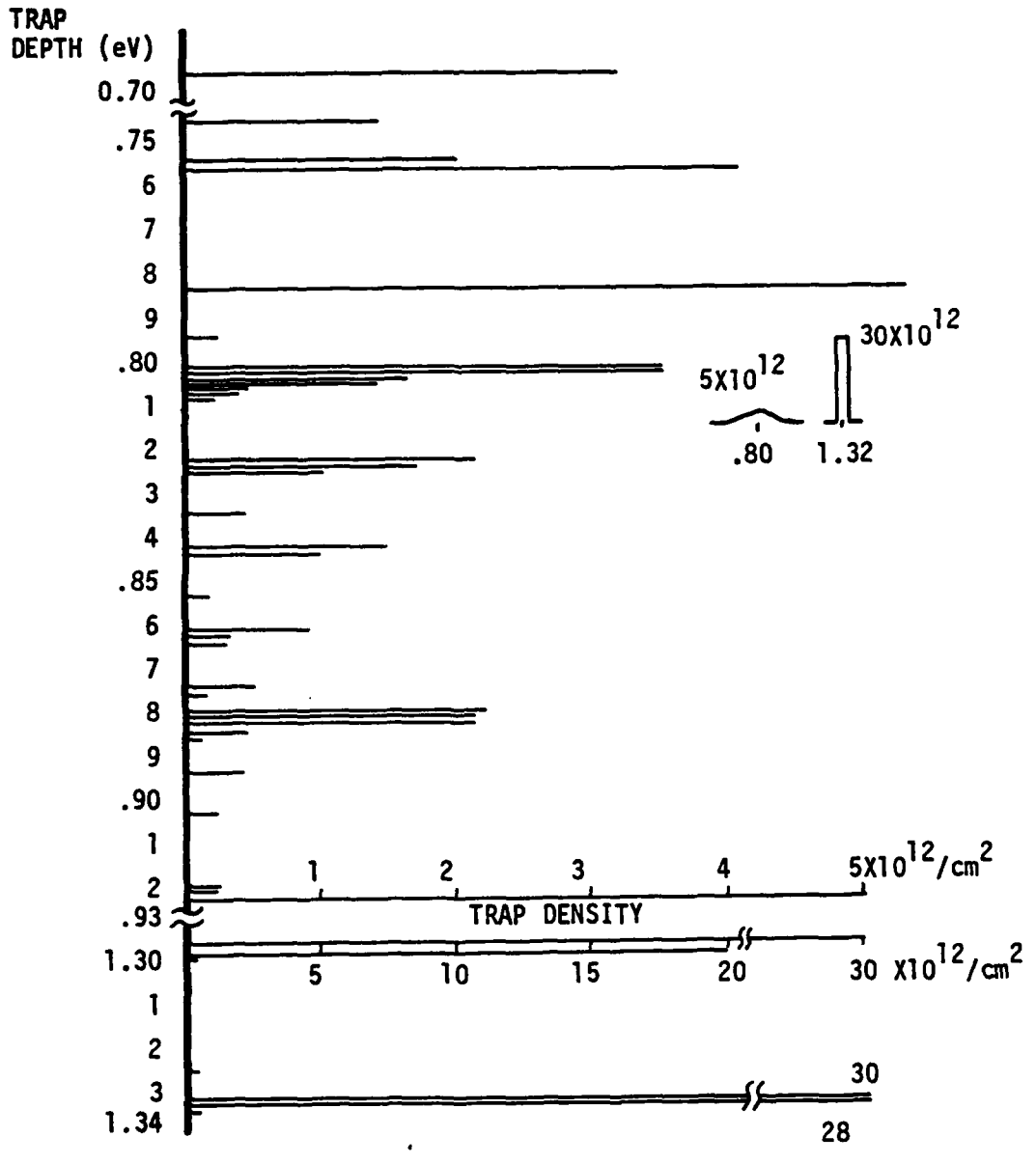


Figure 3-10: Oxide-Nitride Trap Densities

Nitride Bulk Trap Densities

Figures 3-11 through 3-14 show the shallow, medium and deep nitride bulk trap densities. The shallow traps (1.14 to 1.19 eV) exhibit a flat density distribution on the order of 1.5×10^{18} traps per cubic centimeter over the entire energy range as seen in Figure 3-11.

The medium depth (1.35 to 1.58 eV) bulk nitride trap energy range shown in Figure 3-12 can be looked at in three pieces. The 1.35 to 1.37 eV range reaches a density of $1.2 \times 10^{18} cm^{-3}$ centered at 1.36 eV. The 1.40 to 1.43 eV range reaches a density of $1.1 \times 10^{18} cm^{-3}$ at 1.42 eV. The 1.47 to 1.58 eV range has a fairly flat spatial density of $1.0 \times 10^{18} cm^{-3}$.

The data in the deep (1.92 to 2.32 eV) bulk nitride trap energy range is more irregular. Figure 3-13 shows the 1.92 to 2.14 eV range divided into two segments (1.92 to 2.03 eV and 2.06 to 2.14 eV). The trap density appears to increase within each segment, to $8 \times 10^{18} cm^{-3}$ in the 1.92 to 2.03 eV segment and to $3 \times 10^{18} cm^{-3}$ in the 2.06 to 2.14 eV segment. Figure 3-14 shows the 2.15 to 2.32 eV range. Although there are some points which do not conform, there appears to be a gradual increase from 1×10^{18} to $4 \times 10^{18} cm^{-3}$ trap density over the 2.15 to 2.32 eV range. These individual trap densities are similar to an overall bulk nitride trap density of $6 \times 10^{18} cm^{-3}$ for an MNOS structure deduced by Arnett and Yun.[88]

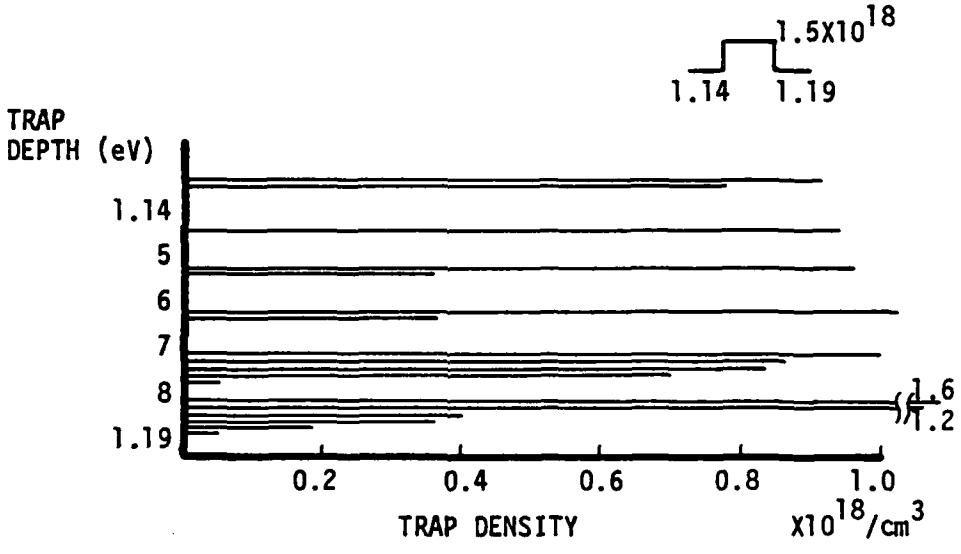


Figure 3-11: Shallow Nitride Bulk Trap Densities

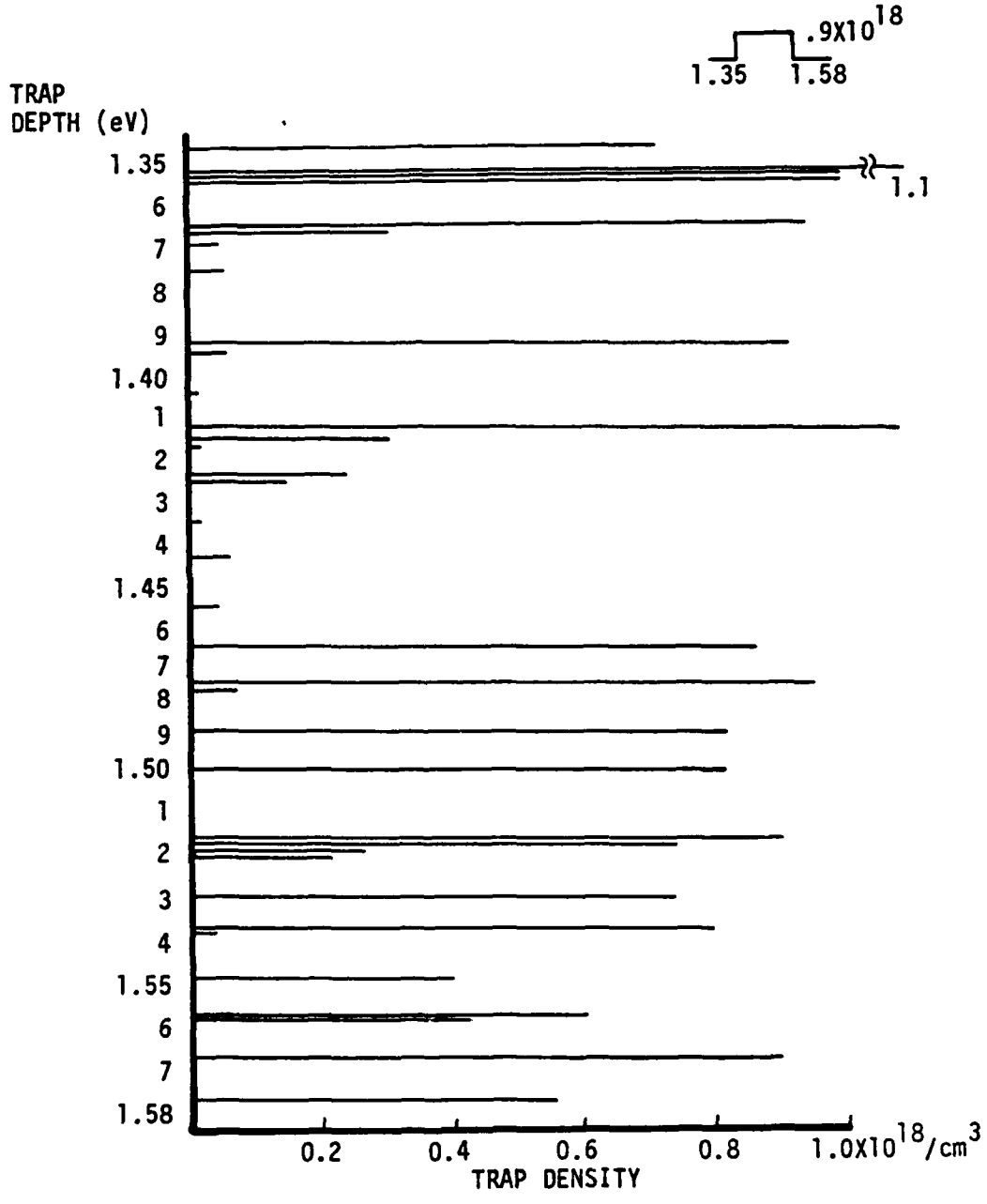


Figure 3-12: Medium Depth Nitride Bulk Trap Densities

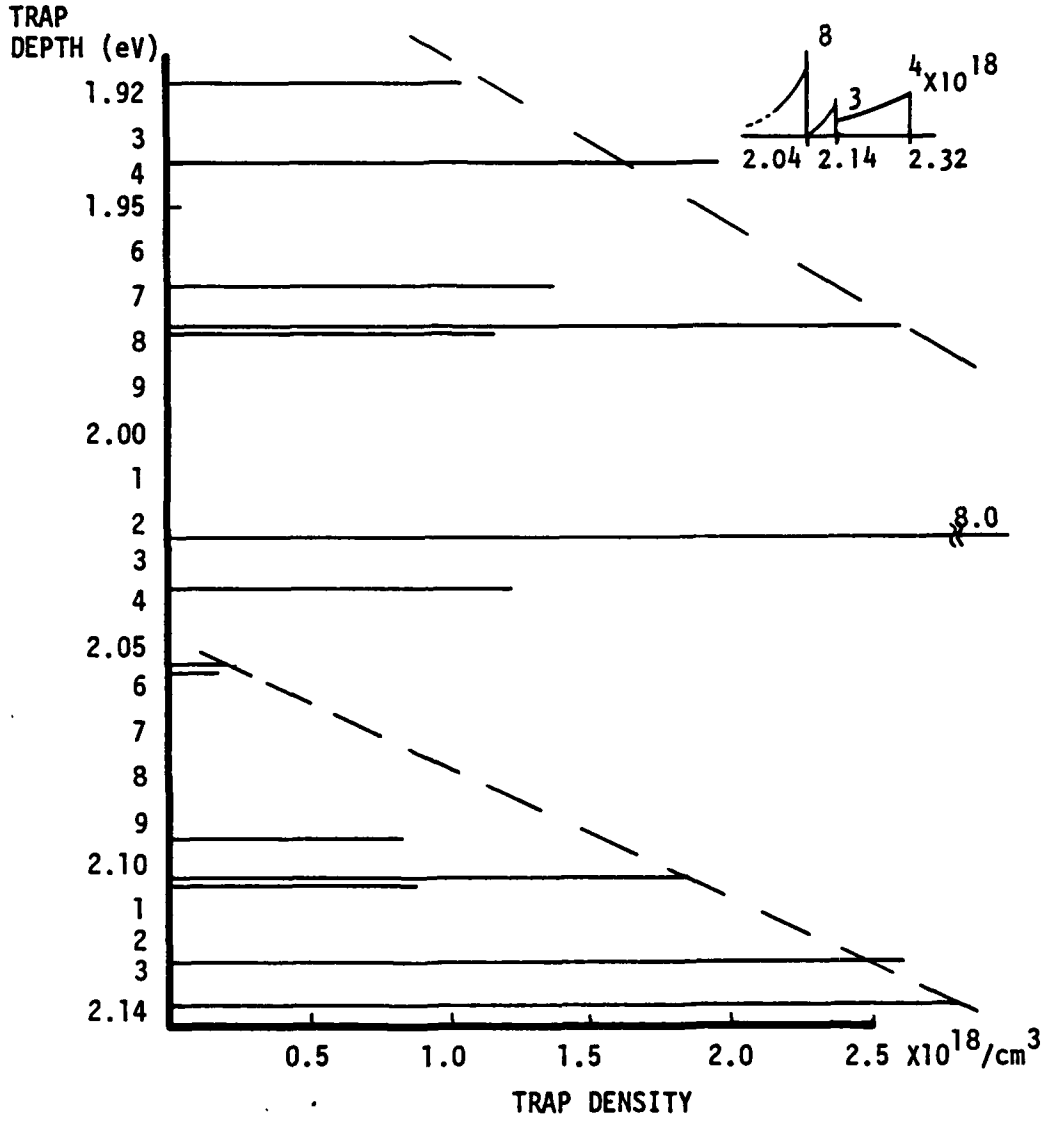


Figure 3-13: Deep (1.92 to 2.14 eV) Nitride Bulk Trap Densities

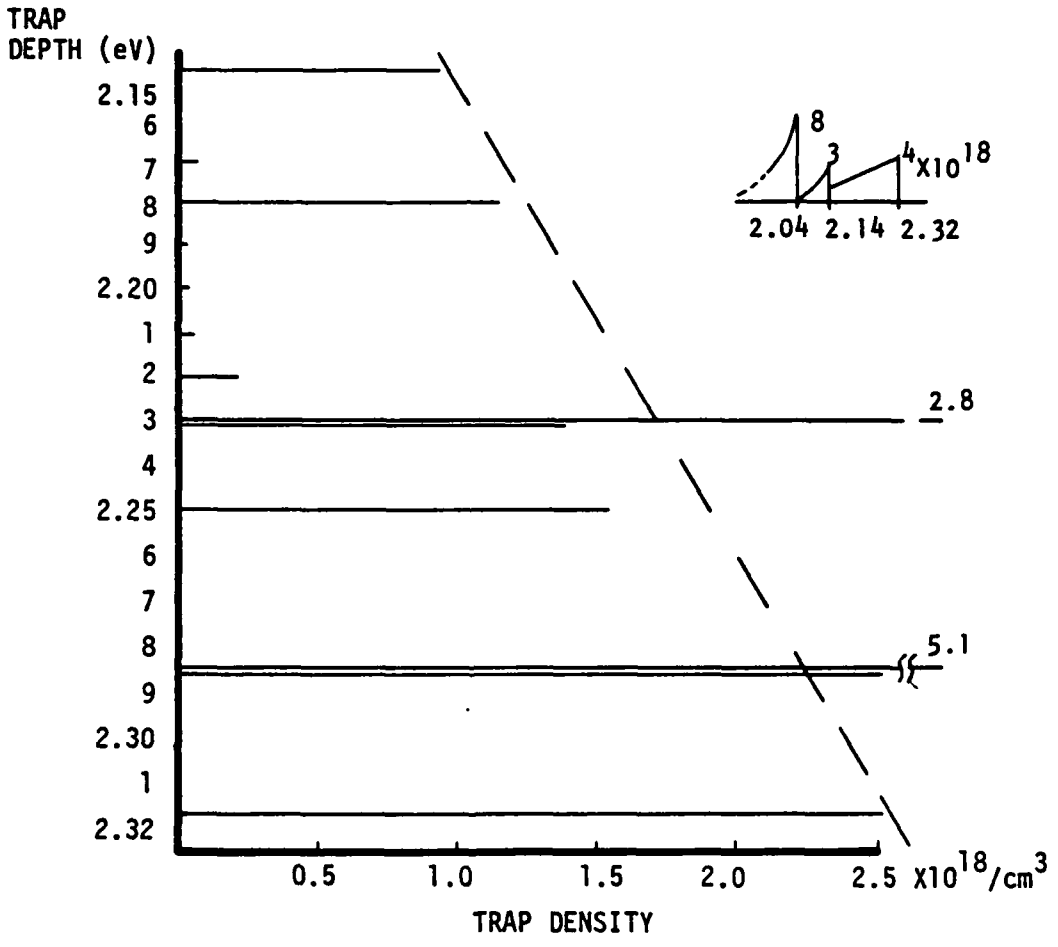


Figure 3-14: Deep (2.15 to 2.32 eV) Nitride Bulk Trap Densities

Silicon-Silicon Oxide Surface States

The results of calculations of surface states fell into two definite groups. Devices which had been subjected to positive and negative bias voltages of 25 volts or less exhibited silicon-silicon oxide surface state densities of less than $0.15 \times 10^{12} cms^{-2}$. Devices subjected to positive or negative bias voltages in excess of 25 volts showed surface state densities of 1 to $5 \times 10^{12} cms^{-2}$. Figure 3-15 shows the "unstressed" devices' low surface state densities clustered around a trap depth 0.4 eV below the silicon conduction band. The "stressed" devices evidenced a wider range of trap depths, and densities up to two orders of magnitude greater than the unstressed. This data is similar to the negative bias stress results of Jeppson and Svensson[53] of $1.2 \times 10^{12} cms^{-2}$ surface state density after a 50 volt stress on MOS structures. Neugebauer and Barnicle[65] also noted "unstressed" device surface state density below $0.3 \times 10^{12} cms^{-2}$ and stressed device surface state density up to $10 \times 10^{12} cms^{-2}$ after extended 20 volt bias stress in MNOS structures.

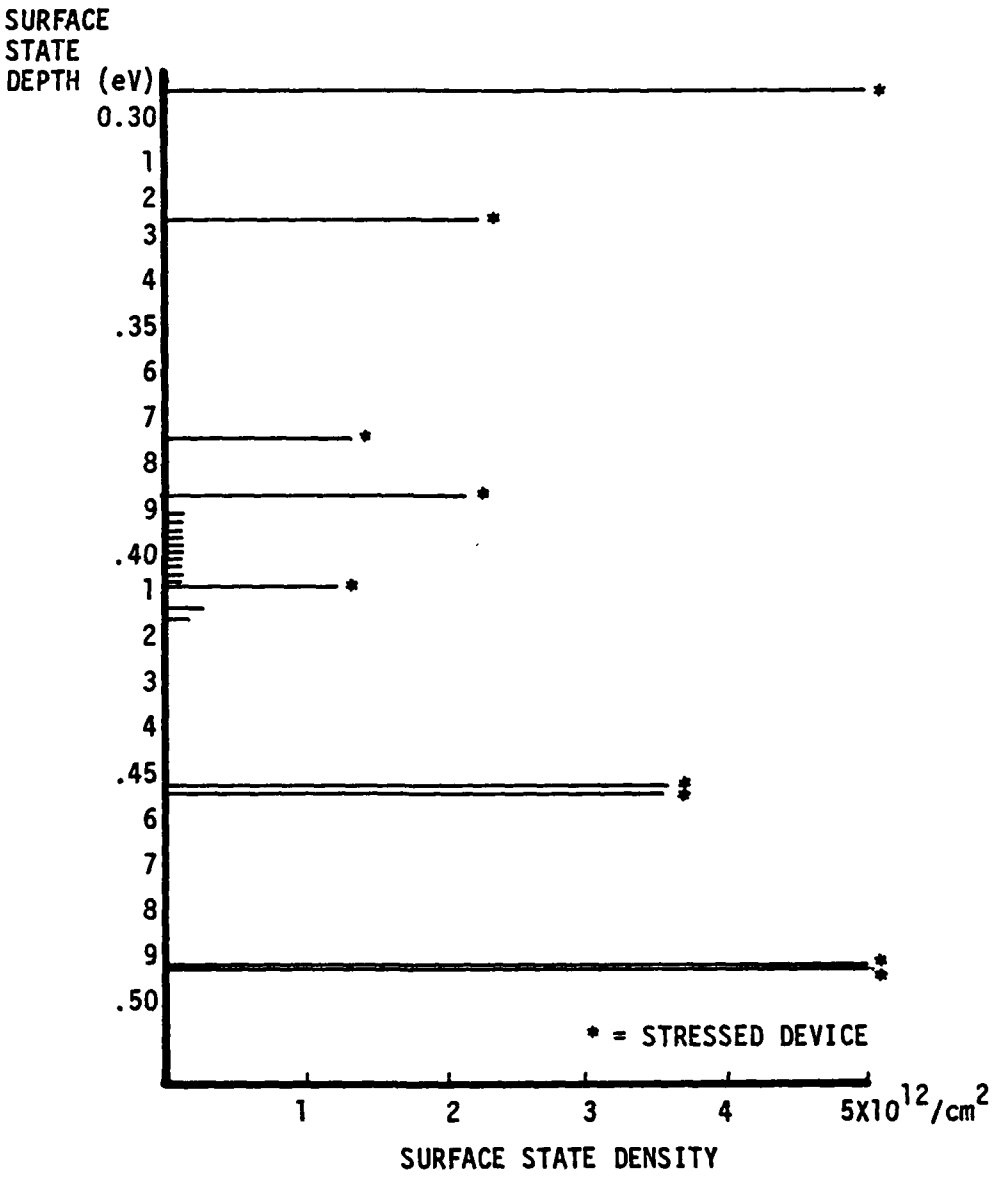


Figure 3-15: Silicon-Silicon Oxide Surface State Densities

Trap Parameter Summary

Trap Location	Trap Depth (eV)	Maximum Trap Density (cm^{-2})	(cm^{-3})
Nitride	1.14 - 1.19	5×10^{12}	1.5×10^{18}
	1.35 - 1.38	5	1.2
	1.40 - 1.43	4	1.1
	1.47 - 1.58	4	1.0
	1.92 - 2.04	32	8.0
	2.05 - 2.14	12	3.0
	2.15 - 2.32	12	4.0
Oxide-nitride	0.70 - 0.93	6	
	1.30 - 1.34	30	
Interface Dopant	1.71 - 1.79	4	
	1.82 - 1.86	6	
Silicon-silicon dioxide	0.3 - 0.5	0.1 (Virgin) 5 (High Field Stressed)	

Table 3-3: Trap Energy Levels and Spatial Densities

3.4.3 Observations

It was noted in Section 2.3.3 that the penetration of the charge centroid, in interface doped MNOS devices under high injected charge conditions, would indicate that the density of bulk nitride traps is sufficiently large that the bulk nitride charge trapping renders the interface dopant trapping neglegible for the high injected charge condition. The TSC data appears to confirm this, demonstrating a $6 \times 10^{12} cms^{-2}$ trap density for the interface dopant traps and a 10 to $30 \times 10^{12} cms^{-2}$ trap density for several bulk nitride trap levels when a 400 angstrom nitride layer is considered.

The evidence of oxide-nitride interface trap levels and medium depth nitride bulk trap levels in the range 1.30 to 1.58 eV (125°C to 205°C zero field charge emission range) explain the generally reported good behavior of the zero bias retention characteristics up into the 125°C to 150°C range.[9, 18, 89]

The interface doped MNOS structures did not exhibit oxide-nitride interface trap or appreciable shallow or medium depth nitride bulk trap emission peaks. The interface dopant is deposited as an evaporated thin film, nominally of monolayer (2.5 to 17 angstrom average) thickness. Ultrathin evaporated metal films have been shown to be discontinuous with the metal in the form of isolated islands.[90, 91, 92, 93, 94] Ultrathin gold films (80 angstroms average thickness) have been shown to be made up of islands on the order of 2×10^{-10} square centimeters in area when deposited on cool substrates.[91, 94] When deposited on elevated temperature substrates the islands tend to coalesce or agglomerate into fewer but larger area bodies. The high temperature evaporation process

caused a definite substrate heating effect. Hence the tungsten dopant (ultrathin, 20 angstrom thick evaporated film) capture cross section would be large, approaching the physical island size ($1.5 \times 10^{-10} cm^2$). The naturally occuring oxide-nitride interface traps would have much smaller capture cross sections. The $20 \times 10^{12} cms^{-2}$ trap density implies a capture cross section on the order of $5 \times 10^{-14} cm^2$. Therefore the probability of charge capture in the oxide-nitride interface trap is much less than in the dopant trap when both are present. To explain the nearly total absence of shallow and medium depth nitride bulk traps, this investigation assumes that the presence of the tungsten dopant influences the nitride growth to the extent that the deep nitride bulk trap development was enhanced over the shallow trap development.

The dopant traps and the deep nitride bulk traps serve to explain some observations made by Neugebauer and Barnicle[65] on interface doped MNOS devices. (1) They noted that both the standard and the doped devices were similar in the charge injection and trapping regime (positive write voltages). This is explained by charging via electron injection from the silicon conduction band through the triangular oxide barrier, to the oxide conduction band and then trapping at the interface (oxide- nitride interface traps or dopant induced traps) and in the nitride. The probability of any trapped hole tunneling from any interface trap to the silicon valence band is less likely because the hole barrier here is the full oxide thickness with a peak height of 5 eV (trap to nitride valence band of at least 3 eV plus 2 eV oxide barrier for holes) versus the 3 eV peak of the thin triangular barrier to silicon conduction band electrons. (2) They noted that for writing at

200°C with 35 volts, a 3.5 volt threshold voltage resulted. When an accelerated retention bias of -15 volts was applied at 200°C the threshold voltage rapidly increased to 6 volts before it started to decrease in the expected fashion. However, for the same voltages at room temperature there was very little increased threshold voltage effect. This can be explained by the 200°C write thermally enhancing the injection of electrons into the nitride bulk. The -15 volt bias created a Poole-Frenkel nitride barrier lowering such that the 1.92 to 2.32 eV nitride trap levels were effectively at 1.32 to 1.72 zero bias levels. This barrier lowering causes detrapping over the 130°C to 245°C range and therfore at the 200°C tenperature there was a rapid detrapping and subsequent redistribution of nitride charges back to the dopant traps. These charges now being closer to the silicon cause a greater effect on the threshold voltage than they did when they were in the nitride bulk. Following this the slower detrapping from the dopant traps and backtunneling from the nitride conduction band into the silicon conduction band occurred. At room temperature there would be slightly less injection into the nitride, but more importantly, at room temperature the nitride will not readily release the trapped charges that are deeper than 1.4 eV (for a -15 volt bias). Therefore no rapid redistribution will occur and the threshold voltage will only be affected by the gradual detrapping and slow backtunneling. (3) They noted that the charge retention characteristics were relatively independent of temperature up to 250°C. The TSC data which locates the dopant traps at 1.71 to 1.86 eV (240°C to 285°C emission temperatures) explain this charge stability.

It has been observed by Yun that there is a very rapid initial decay of stored charge in standard MNOS devices. The shallow oxide-nitride interface traps (0.70 to 0.93 eV) are proposed here as the primary means for this rapid initial stored charge decay. At zero bias these traps empty rapidly at room temperature conditions.

3.4.4 Related Efforts

There have been two previously reported efforts to use TSC techniques to determine trap parameters in standard MNOS devices, those of Katsube, Adachi and Ikoma [95] and those of Simmons, et al. [96, 97] Katsube assumed a discharge model consisting of a sequential phenomena of tunneling of charges from the oxide-nitride interface into silicon-silicon oxide interface states followed by thermal emission from the silicon-silicon oxide interface states into the silicon conduction band. They did not address detrapping from nitride bulk traps (shown in Chapters 1 and 2 to be important) nor did they consider emission into the nitride conduction band followed by tunneling through the oxide. Using curve fitting, they concluded that there were traps 2.55 eV below the nitride conduction band, extending 50 angstroms from the oxide-nitride interface into the nitride.

Their data (Figures 1 to 4, Reference [95]), when subjected to the analysis techniques described in this chapter yield silicon-silicon oxide surface states 0.45 to 0.50 eV below the silicon conduction band, shallow oxide-nitride interface traps 0.95 eV below the nitride conduction band and shallow (1.04 to 1.20 eV) and medium depth (1.42 to 1.61 eV) nitride bulk trapping levels. Thus their TSC data support the findings of this effort.

Wei and Simmons and Mar and Simmons were examining techniques for studying the silicon-silicon oxide interface states and using the MNOS structure as a vehicle because it exhibits a large density of interface states. In the process they observed TSC results attributable to release of MNOS "memory" charges from the oxide-nitride interface or from the nitride bulk. They did not report a determination of trap depth from their data. Applying the analysis of this chapter to their data (Figures 2,3 and 5, Reference[96]) yields a trap level 1.2 eV below the nitride conduction band, placing it in the shallow nitride trapping level range determined from this study.

Some photodepopulation studies of charged MNOS devices have been performed by DiStefano et al.[98, 99] They report only one nitride trapping level, 3 eV below the nitride conduction band. This is in conflict with the results of this work and others and it would imply that the charged MNOS device would be stable and not suffer appreciable retention degradation at temperatures over 500°C. This is also contrary to all reported studies of retention in MNOS devices. Therefore it is assumed that some other interpretation of their data should be made. This study did not attempt to explain their photodepopulation experimental data.

4. CHAPTER FOUR - MODEL VERIFICATION

A model of the interface doped MNOS structure including the trap energy and spatial structure, charge injection and trapping mechanisms and discharge and charge removal mechanisms has been developed. This model, depicted in Figures 4-1, 4-2 and 4-3, was exercised on an HP 2100A minicomputer. For these computations the nitride was divided into ten segments and calculations of the charge conduction, trapping and detrapping as it passed through the oxide and each segment of the nitride were made. Calculations of charge centroid location versus injected charge and threshold voltage shift as a function of write/erase pulse duration and voltage were made and plotted. Comparisons with measured centroid and measured threshold voltage shift data were made.

4.1 Model Description

4.1.1 Energy Band Model of Interface Doped MNOS Structures

The energy band and trap configuration of the interface doped MNOS model is shown in Figure 4-1. This was constructed by simplifying the multilevel trap results shown in Table 3-3, page 122.

The shallow oxide-nitride interface traps are ignored. Their density is much less than the deep oxide-nitride interface trap density and, since they fall in the range of 0.7 to 0.9 eV below the nitride conduction band, any occupied trap will be emptied rapidly above 10^{o}C. The deep oxide-nitride interface traps are represented by a single trap level 1.25 eV below the nitride conduction band. The interface dopant induced trapping levels are represented by a single trap level 1.7 eV below the nitride conduction band. The shallow (1 eV) nitride bulk

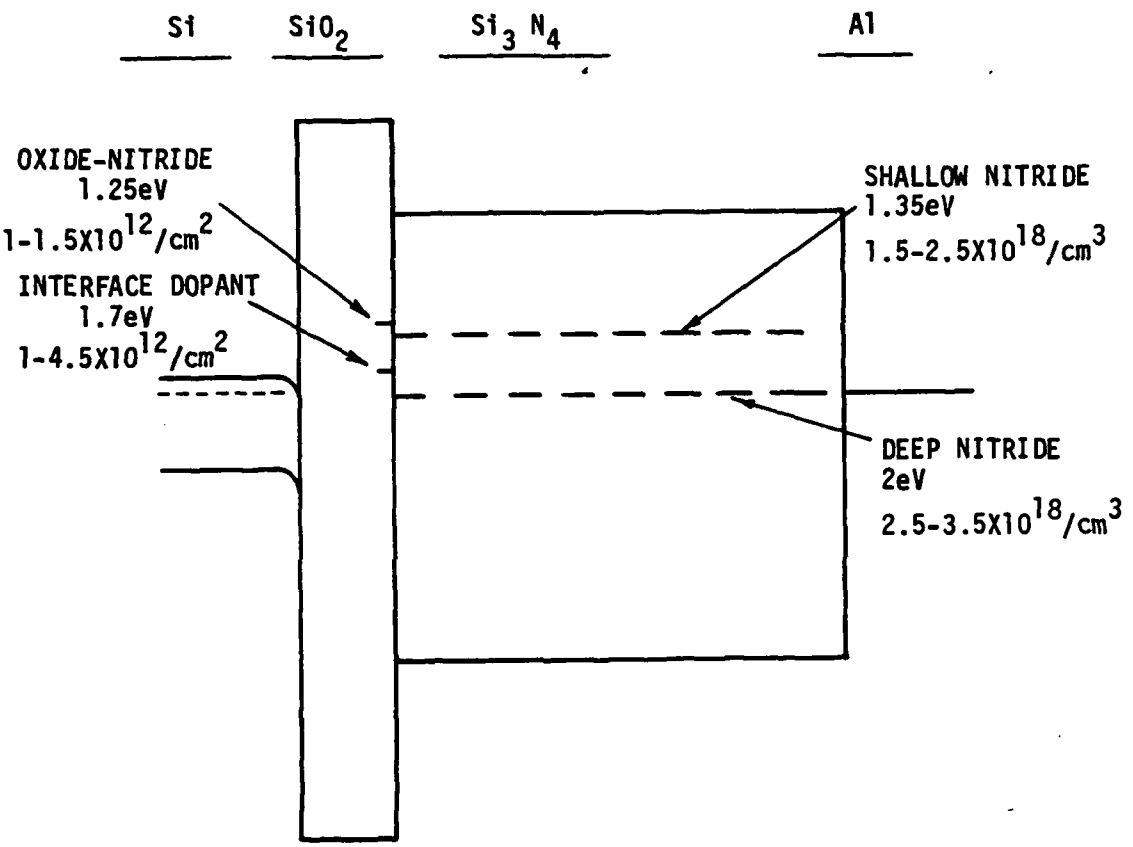


Figure 4-1: Energy Band Model of Interface Doped MNOS Structure

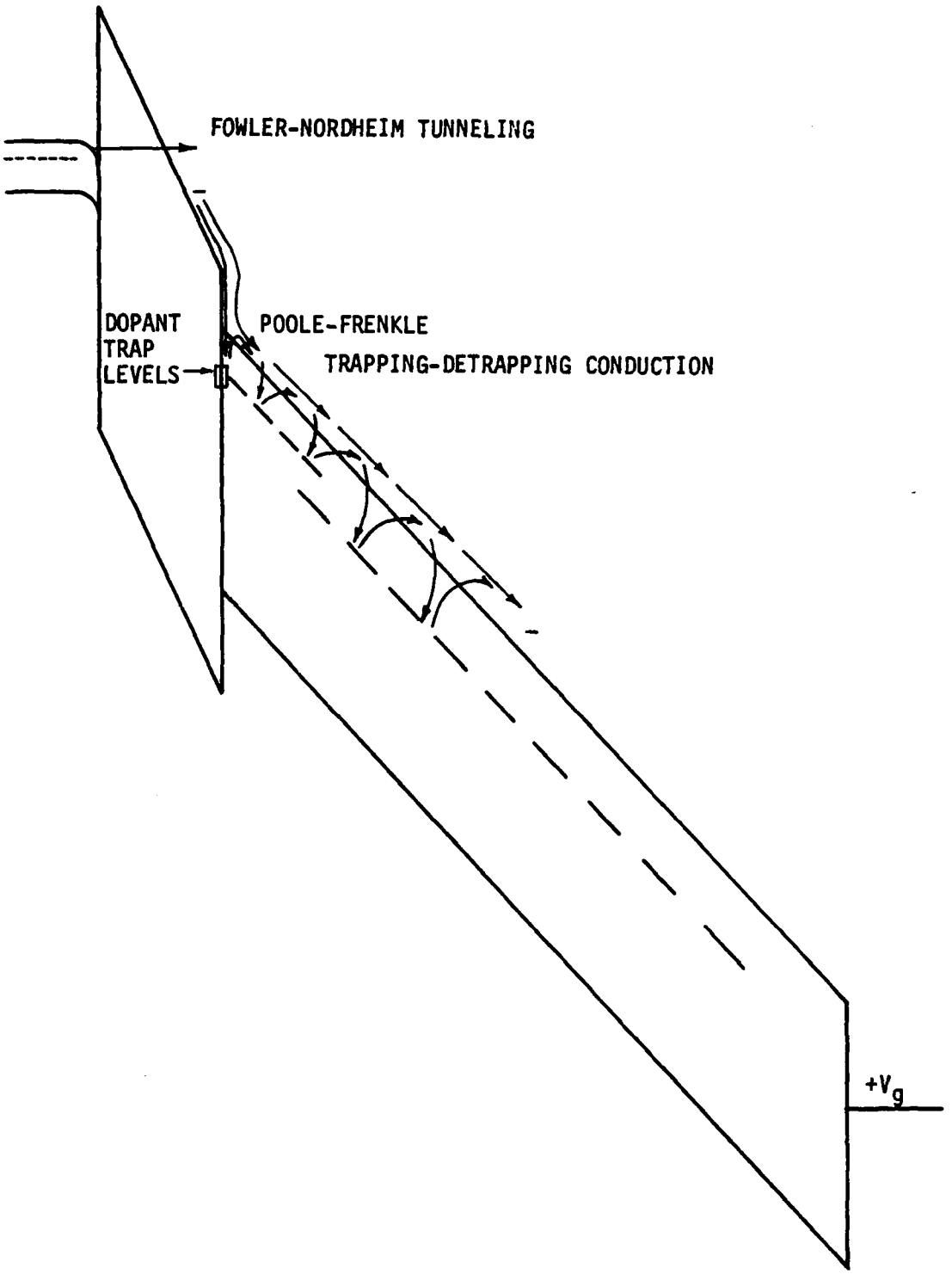


Figure 4-2: Charge Injection Process in Interface Doped MNOS Structures

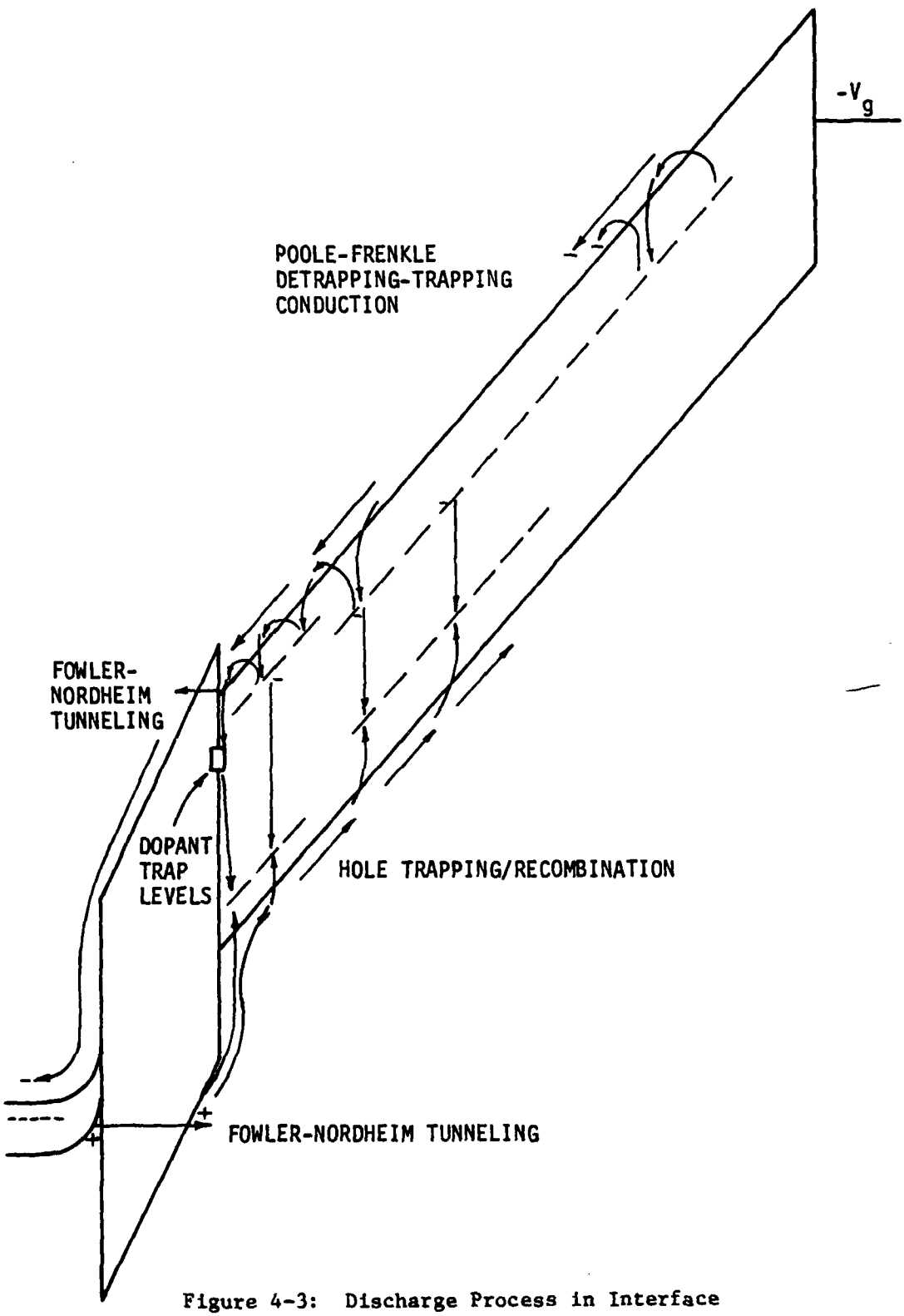


Figure 4-3: Discharge Process in Interface Doped MNOS Structures

traps are also ignored due to their proximity to the nitride conduction band level and the resultant lack of participation in charge trapping at normal room temperature operating conditions. The medium depth bulk nitride trap levels are represented by a single trap level 1.35 eV below the nitride conduction band. The deep bulk nitride trap levels are represented by a single trap level 2 eV below the nitride conduction band. Mathmatically, the model is configured with the deep and shallow nitride traps occupying alternate segments of the nitride layer. This was done to simulate, in a simple form, a uniform distribution of deep and shallow traps throughout the nitride. The selection of the values for each of these single trap levels for demonstrating the model is in consonance with the trap depths determined by TSC analysis and the simplification is necessary to make calculations of charging and discharging effects manageable.

The trap densities used in the model reflect the TSC trap density measurement results of Chapter 3. The specific values used are shown on Figure 4-1 and in Tables 4-1 and 4-2.

4.1.2 Charge Injection Process

Charge transfer under positive gate bias (device writing) results in an increase in the negative charge in the MNOS traps for the customary or "forward" write conditions. For this model the charge transfer was taken to be injection of electrons from the silicon conduction band. The other possible charge movements which could result in increased negative charge in the MNOS insulators are injection of electrons from the silicon valence band and ejection of holes from the nitride valence band into the silicon. Electron injection from the

valence band was rejected because the tunneling barrier height and thickness are both much greater than for electron injection from the conduction band. Hole ejection from the nitride valence band was rejected because the highly non-conductive nature of the nitride indicates that there is a very low density of free electrons or holes in the nitride thereby preventing appreciable hole tunneling from the nitride valence band.

Figure 4-2 shows the ideal energy band structure to scale when a typical gate bias of 19 volts is applied to an 80 angstrom oxide/400 angstrom nitride aluminum gate MNOS device. Charge injection from the silicon must be by Fowler-Nordheim tunneling from the silicon conduction band into the oxide conduction band. The electrons then proceed under the influence of the oxide electric field through the oxide toward the oxide-nitride interface. Section 4.1.4 details the Fowler-Nordheim tunneling equation used to express the oxide electron current. For the purpose of computer simulation a charge "packet" was formed by the product of oxide electron current and write pulse duration. This "packet" then traversed the nitride interacting with traps at the oxide-nitride interface and then with the nitride traps, one nitride segment at a time.

At the oxide nitride interface a portion of the electron charge packet is trapped in interface dopant induced traps or in oxide-nitride interface traps, depending on whether the device has an interface doped MNOS or conventional MNOS structure, respectively. The number of charges trapped is proportional to the trap capture cross section, number of empty traps and number of charges in the packet. The trapping

expression is detailed in Section 4.1.4.

Simultaneously, trapped electrons are emitted from the oxide-nitride interface via a Poole-Frenkel type field assisted thermal excitation into the nitride conduction band. The number of detrapped charges is proportional to write pulse duration, number of trapped charges, attempt-to-escape frequency and an exponential function of trap depth and electric field. The expression used for the detrapping is detailed in Section 4.1.4.

Electrons in the nitride conduction band undergo a trapping/detrapping process through the nitride layer, determined by the nitride trap parameters, trap occupancy, temperature and electric field. For the computer implementation of the model, the nitride current trapping/detrapping process was simulated by following the oxide electron current charge packet as it passed through each of the ten nitride segments, interacting with the traps and trapped electrons. The portion of the oxide electron current charge packet that was <u>not</u> trapped at the interface plus the electrons detrapped from the oxide-nitride interface form the charge packet which enters nitride segment one. A portion of this new packet will be trapped and some previously trapped electrons will be detrapped from segment one. Thus a new packet is formed to enter nitride segment two. This procedure is followed for all ten nitride segments. After the charge packet interaction with the traps in the last nitride segment, any electrons remaining in the nitride conduction band are assumed to pass out through the gate contact.

4.1.3 Discharge Process

Charge transfer under negative gate bias (device erasure) results in a decrease in the negative charge stored in the MNOS traps. A much more complex charge transfer process for the erase mode was required to explain experimentally measured threshold voltage characteristics. This can be seen in Figure 4-3.

Holes are injected from the silicon valence band, through the oxide, into the oxide valence band. The Fowler-Nordheim type charge injection expression detailed in Section 4.1.4 is used to express the oxide hole current. The holes then proceed in the oxide valence band to the oxide-nitride interface. Here also, for simulation purposes, the product of oxide hole current and erase pulse duration is used to form an injected charge packet.

At the oxide-nitride interface a portion of the hole packet is trapped via direct recombination with trapped electrons. The trapping is proportional to trap capture cross section, number of trapped electrons and number of charges in the hole packet. Because this event is considered to involve recombination, no hole detrapping process is considered.

Injected, non-trapped, holes remaining in the nitride valence band undergo trapping and recombination with trapped electrons while traversing the nitride toward the gate. Interaction with the trapped electrons in each of the ten nitride segments is considered sequentially. Again, only hole trapping/recombination is considered in each nitride segment. Any portion of the hole packet which has not

undergone trapping/recombination by the time it has interacted with the tenth nitride segment is assumed to contribute to the gate current.

Simultaneously, electrons undergo Poole-Frenkel detrapping and retrapping processes, traversing the nitride, via the conduction band, toward the oxide-nitride interface. For simulation purposes the ten segment nitride approach is used, starting with electron detrapping from the segment adjacent to the gate (segment ten). These electrons, detrapped during the erase pulse duration, form the electron charge packet which enters segment nine. Electrons will be detrapped from segment nine. A portion of the electron charge packet which entered segment nine will be retrapped. The portion of the electron charge packet which entered segment nine but was <u>not</u> retrapped, plus the segment nine detrapped electrons, form the electron charge packet which enters segment eight. This detrapping/retrapping is continued for each nitride segment. The trapping and detrapping expressions are detailed in Section 4.1.4.

At the oxide-nitride interface some trapped electrons are excited out of the interface and some of the electrons released from bulk nitride traps into the nitride conduction band will be retrapped at the interface. The detrapped interface electrons and the bulk nitride trap electrons remaining in the nitride conduction band participate in a Fowler-Nordheim type tunneling from the nitride conduction band, through the oxide into the oxide conduction band and then into the silicon conduction band.

4.1.4 Theoretical Expressions and Model Parameters

Fowler-Nordheim Injection

Fowler-Nordheim injection is tunneling of carriers through an insulator triangular energy barrier into the free carrier band of the insulator. In the MIS structure of the model this was electron injection from the silicon conduction band through the oxide energy barrier into the oxide conduction band under positive gate bias; electron injection from the nitride conduction band through the oxide energy barrier into the oxide conduction band under negative gate bias; and hole injection from the silicon valence band through the oxide energy barrier into the oxide valence band under negative gate bias. This is shown in Figures 4-2 and 4-3. The expression for Fowler-Nordheim injection is of the form:[24, 85]

$$J = (q^2F_{ox}^2/8h\pi\phi_B)\exp-[8\pi(2m^*q)^{1/2}\ \phi_B^{3/2}/3hF_{ox}] \qquad (4.1)$$

where J = electron or hole current density

F_{ox} = oxide electric field

ϕ_B = $Si-SiO_2$ conduction band barrier (3.1 eV) Ref[9]

$Si-SiO_2$ valence band barrier (3.8 eV) Ref[9]

$Si_3N_4-SiO_2$ conduction band barrier (1.03 eV) Ref[9]

m^* = electron or hole effective mass (.42*m) Ref[24, 85]

The n-type silicon-silicon oxide conduction band barrier is modified by the image force effect for electrons undergoing Fowler-Nordheim injection from the silicon conduction band. The reduction in the barrier height is calculated[71] from Equation (4.2).

$$\Delta\phi_B = (qF_{ox}/4\ \pi\varepsilon_{ox})^{1/2} \tag{4.2}$$

Poole-Frenkel Detrapping

Poole-Frenkel conduction is an electric field assisted, thermal emission process. In the MIS structure of the model this occurred in the bulk nitride and involved excitation of electrons from nitride bulk traps, oxide-nitride interface traps and interface dopant induced traps into the nitride conduction band. The expression for the number of charges detrapped during a time period Δt is a strong function of the trap depth, electric field and Poole-Frenkel constant and is of the form:[81, 84, 100, 101]

$$\Delta n_t = \Delta t\ n_t\ \nu\ \exp-[(q/kT)(E_t - \beta F^{1/2})] \tag{4.3}$$

where Δn_t = number of detrapped charges
(cm^{-2} at interface, cm^{-3} in nitride)

n_t = number of charges in traps
(cm^{-2} at interface, cm^{-3} in nitride)

ν = attempt-to-escape frequency (Equation (3.2))

E_t = trap depth

β = Poole-Frenkel constant

F = nitride electric field at the trap location

Substituting expressions from Equation (3.2), the number of charges detrapped during a time period Δt is:

$$\Delta n_t = \Delta t \; n_t \sigma m^* (4\pi)^{3/2} \sqrt{\frac{3}{2}} \, h^{-3} \, (kT)^2 \exp-[(q/kT)(E_t - \beta F^{1/2})] \qquad (4.4)$$

where σ = trap capture cross section for electrons
m^* = electron effective mass
T = temperature

The values of capture cross section used in the model were proportional to the trap density. The nitride bulk deep trap density was on the order of 3×10^{18} traps per cubic centimeter. The corresponding trap volume reduces to a physical cross section of 5×10^{-13} square centimeters. The value of carrier capture cross section used in the model for the bulk nitride deep traps was 1×10^{-14}

square centimeters. The nitride bulk shallow trap density was on the order of 1×10^{18} traps per cubic centimeter. The corresponding trap volume reduces to a physical cross section of 1×10^{-12} square centimeters. The value of carrier capture cross section used in the model for the bulk nitride shallow traps was 1×10^{-13} square centimeters. This is comparable to the value of 5×10^{-13} measured by others [88, 102] for this type of nitride trap. The oxide-nitride interface trap density was on the order of 2×10^{12} traps per square centimeter. This corresponds to a cross section of 3×10^{-13} square centimeters. The value of capture cross section used in the model for the oxide-nitride interface traps was 5×10^{-14} square centimeters. The capture cross section of the interface dopant induced trap was based on the ultrathin film "island" size. The island size was shown in Section 3.4.3 to be on the order of 1.5×10^{-10} square centimeters. The value of electron capture cross section used in the model was 2.5×10^{-12} square centimeters. The hole capture cross section was much larger because the trapping site was negatively charged by trapped electrons. The value used in the model was 2.5×10^{-10} square centimeters.

The theoretical value of the Poole-Frenkel constant, calculated from Equation (3.8), is 3×10^{-4} $(Vcm)^{1/2}$ for a silicon nitride film with a relative dielectric constant of 7. Values of Poole-Frenkel constant reported by other investigators [14, 23, 29, 40, 83, 103] based on measurements on thin silicon nitride films have been in the range 1.6 to 4.3×10^{-4} $(Vcm)^{1/2}$. The value 2.9×10^{-4} $(Vcm)^{1/2}$ was used in the model.

Charge Trapping

The portion of the charge packet that was trapped during interaction with traps at the interface or in a nitride segment is given by:

$$\Delta Q_p = Q_p \sigma (N_t - n_t) \tag{4.5}$$

where ΔQ_p = density of charges trapped from charge packet (cm^{-2} at interface, cm^{-3} in nitride)

σ = trap capture cross section

N_t = trap density (cm^{-2} at interface, cm^{-3} in nitride)

n_t = density of charges in traps (cm^{-2} at interface, cm^{-3} in nitride)

Q_p = density (cm^{-2}) of charges in packet interacting with nitride segment traps or at an interface

4.2 Comparison of Calculated and Measured Characteristics

4.2.1 Charge Centroid Data Comparison

As described in Chapter 2, charge injection versus charge centroid data was determined in this study from measurements on MNOS structures having four variations of oxide thickness and interface dopant density. The device parameters were described in Section 2.3.

The charge centroid measurements were made under writing, or electron injection, conditions. The model was exercised for each of the

device types with positive polarity (write) pulses of various amplitudes and durations. For each pulse, the calculated injected charge distribution was used to calculate the charge centroid using Equation (2.15) and the calculated injected charge versus charge centroid curves were plotted.

From the data shown plotted in Figures 2-17 through 2-20, straight line segment approximations to the measured injected charge versus charge centroid relations were determined and plotted along with the calculated values in order to compare the model's results.

Figures 4-4 through 4-7 show the centroid versus injected charge curves as calculated by the model (solid line) and as measured (dotted line). The parameters used in the model for each device are shown in Table 4-1.

Figures 4-8 and 4-9 show the calculated threshold voltage shift (solid curve) under the conditions of these charge centroid calculations for an interface doped device and a conventional, no dopant, device respectively. Also shown are the measured threshold voltage shifts (dotted curve) from this study.

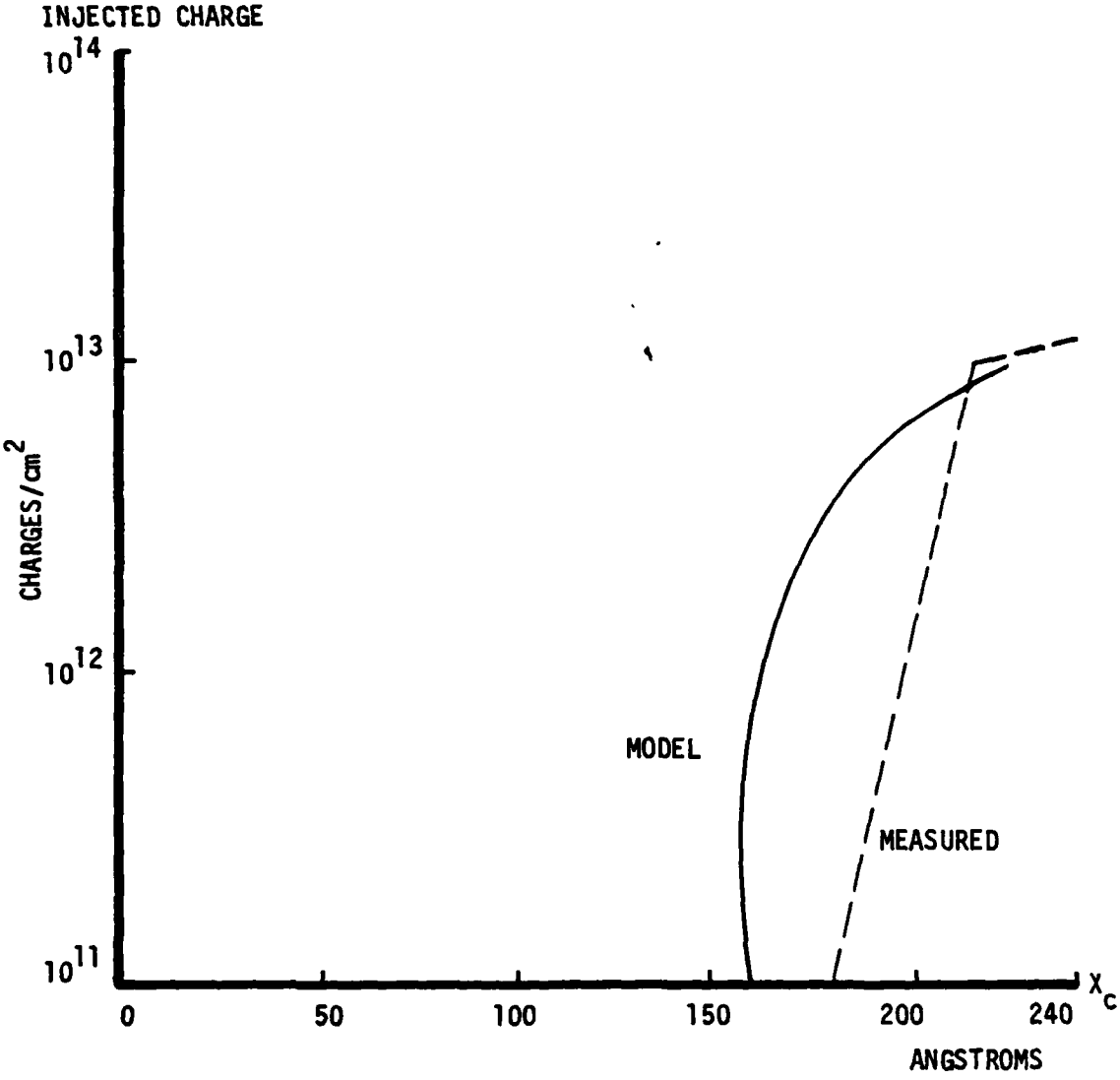


Figure 4-4: Injected Charge Versus Charge Centroid for MNOS Structure.

No Interface Dopant. Oxide/Nitride Thickness: 32/468 Angstroms. Calculated (solid line). Measured (dotted line)

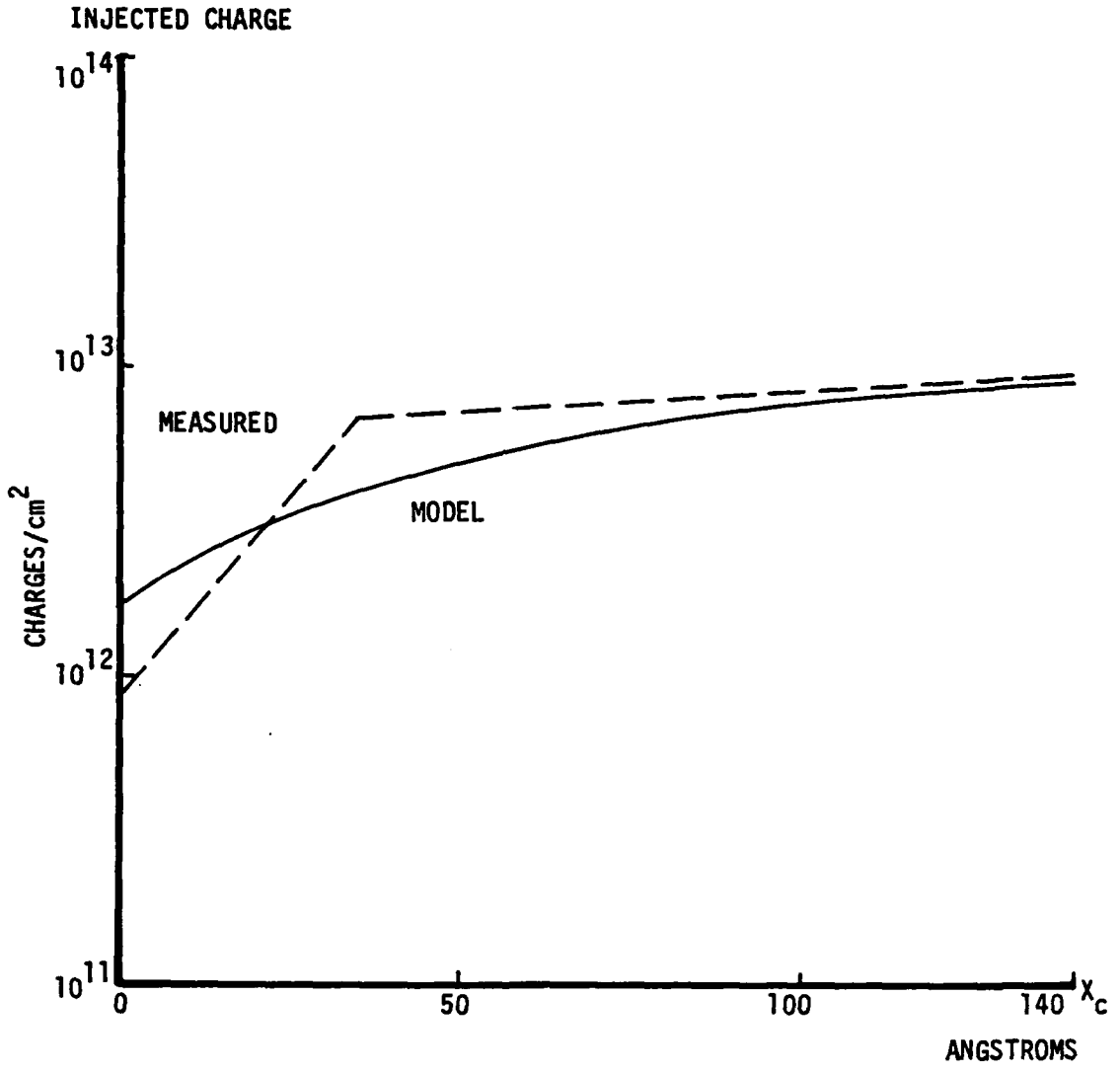


Figure 4-5: Injected Charge Versus Charge Centroid for DMNOS Structure. 3×10^{14} cm^{-2} Dopant Density. Oxide/Nitride Thickness: 32/515 Angstroms. Calculated (solid line). Measured (dotted line)

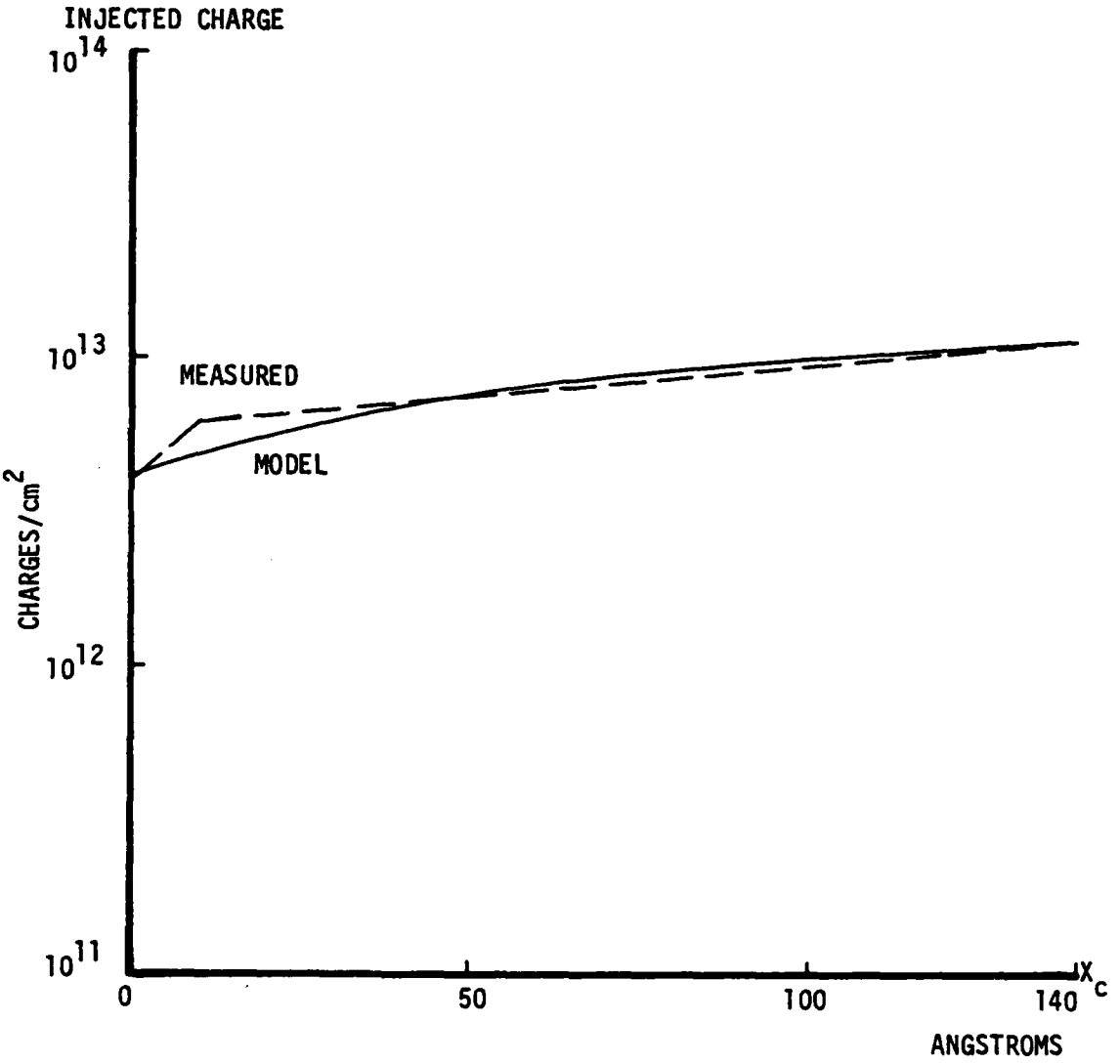


Figure 4-6: Injected Charge Versus Charge Centroid for DMNOS Structure. 2×10^{15} cm^{-2} Dopant Density. Oxide/Nitride Thickness: 32/468 Angstroms. Calculated (solid line). Measured (dotted line)

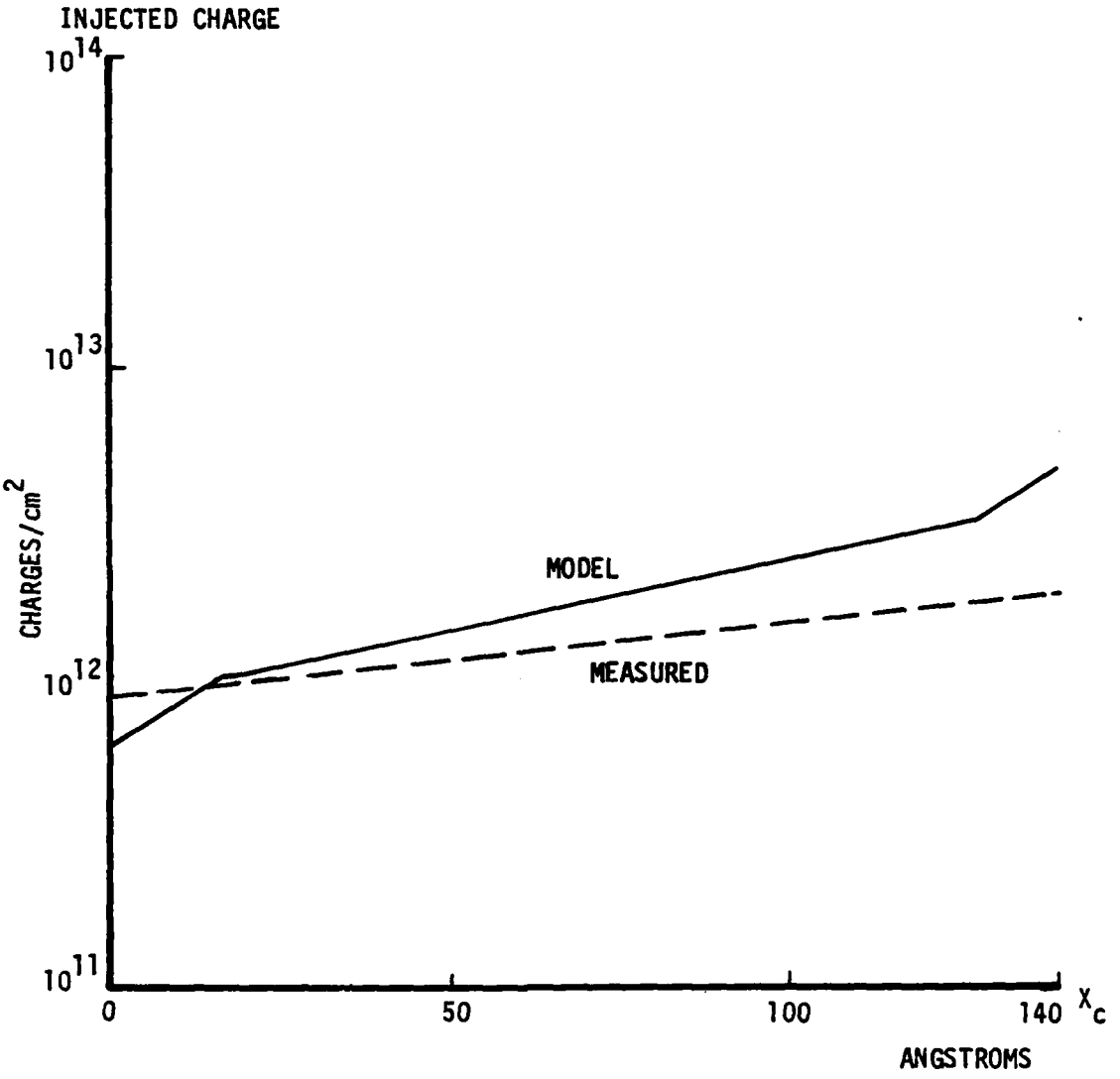


Figure 4-7: Injected Charge Versus Charge Centroid for DMNOS Structure.

3×10^{14} cm^{-2} Dopant Density. Oxide/Nitride Thickness: 52/468 Angstroms. Calculated (solid line). Measured (dotted line)

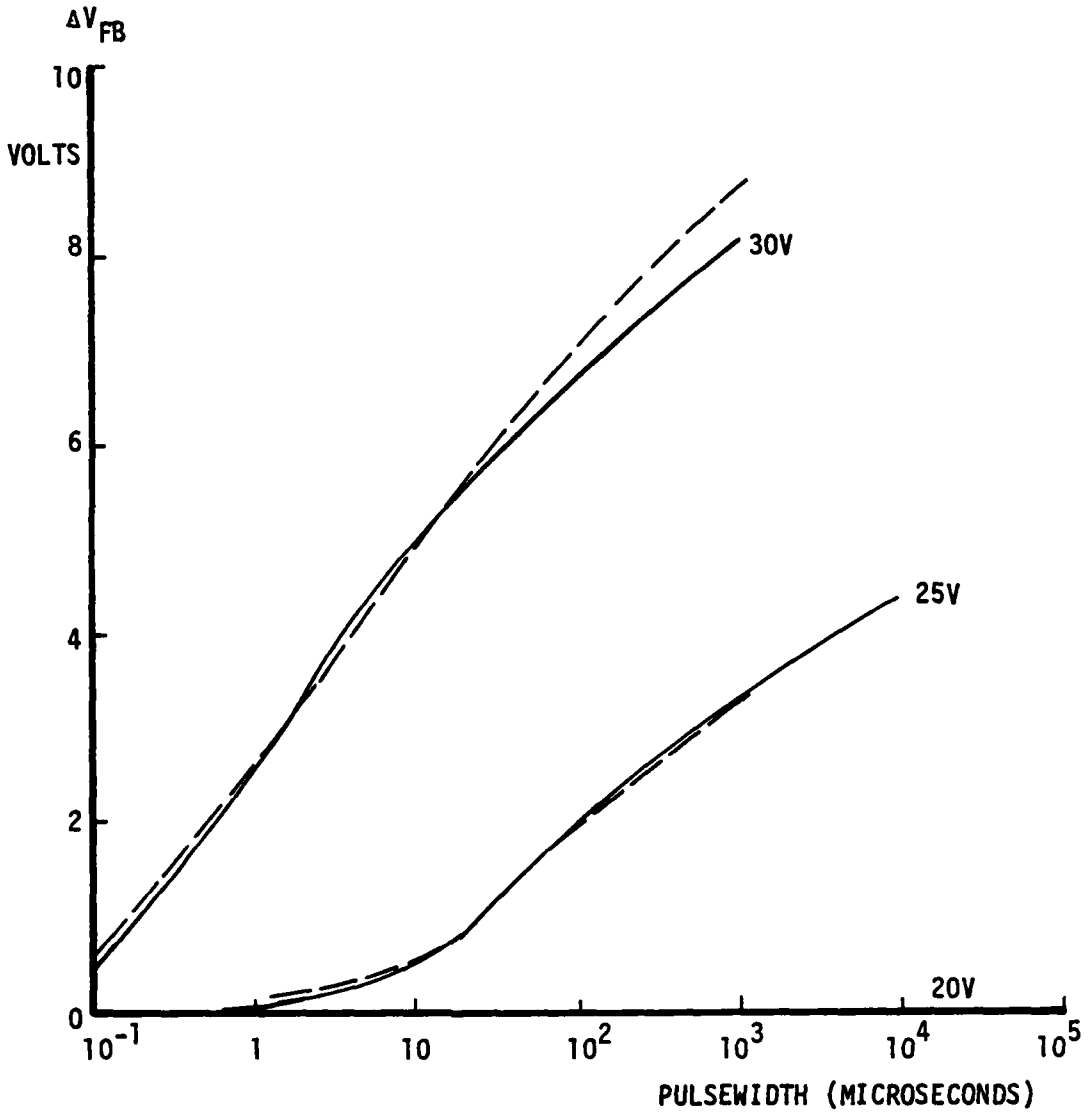


Figure 4-8: Write Characteristics: 0.3 x 10^{15} cm^{-2} Dopant Density

32 angstrom oxide, 515 angstrom nitride.
Calculated curves (solid). Measured data (dotted).

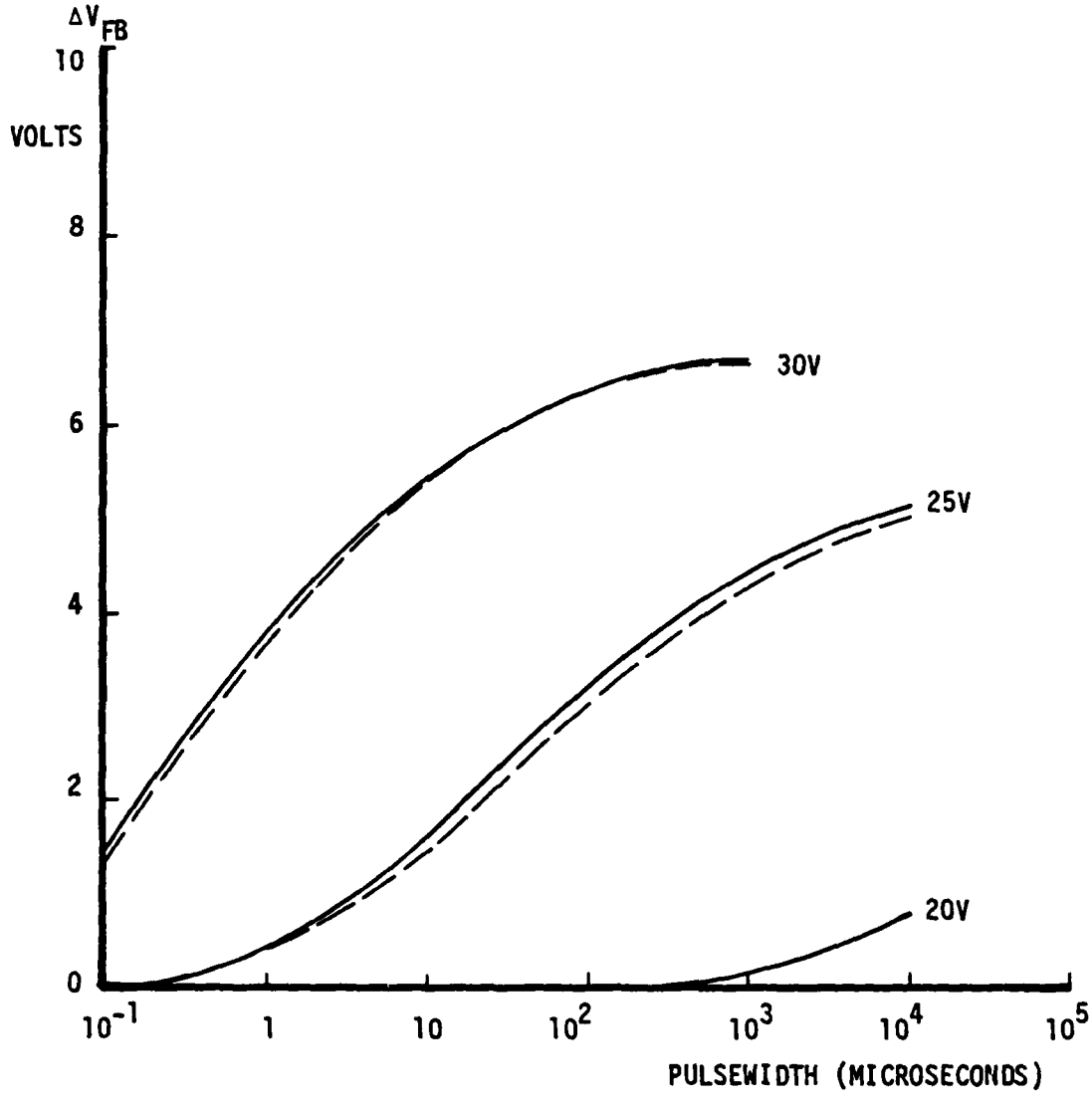


Figure 4-9: Write Characteristics - No Interface Dopant

32 angstrom oxide, 468 angstrom nitride.
Calculated curves (solid). Measured data (dotted).

Observations

The model does not provide an exact prediction of charge centroid as a function of injected charge. However, it does reproduce the form of the injected charge versus charge centroid curve. It predicts a deep charge centroid for the conventional MNOS structure, and it predicts the near zero charge centroid for low levels of injected charge followed by penetration of the centroid into the nitride at higher levels of injected charge. Figures 4-8 and 4-9 demonstrate that the write characteristics can be closely predicted in spite of the deviation from the measured charge centroid characteristic. The threshold voltage shifts, although related to the charge centroid-injected charge relation, do not appear to have a sensitive or critical dependency.

4.2.2 Write/Erase Characteristics Comparison

Write and erase characteristics for thick oxide MNOS devices having no interface dopant and a high density of tungsten interface dopant (1.5×10^{15} cm^{-2}) have been reported by Neugebauer and Barnicle.[65] The model was exercised using their oxide and nitride thickness parameters and an appropriate value for interface dopant trap density. The plots of calculated threshold voltage shift versus write/erase pulse width for several write/erase voltages are shown in Figures 4-10 through 4-13. The measured data points from Neugebauer are also shown. The values of capture cross section, trap densities, trap depths and Poole-Frenkel constant used in the model for these calculations for the two types of devices are shown in Table 4-2.

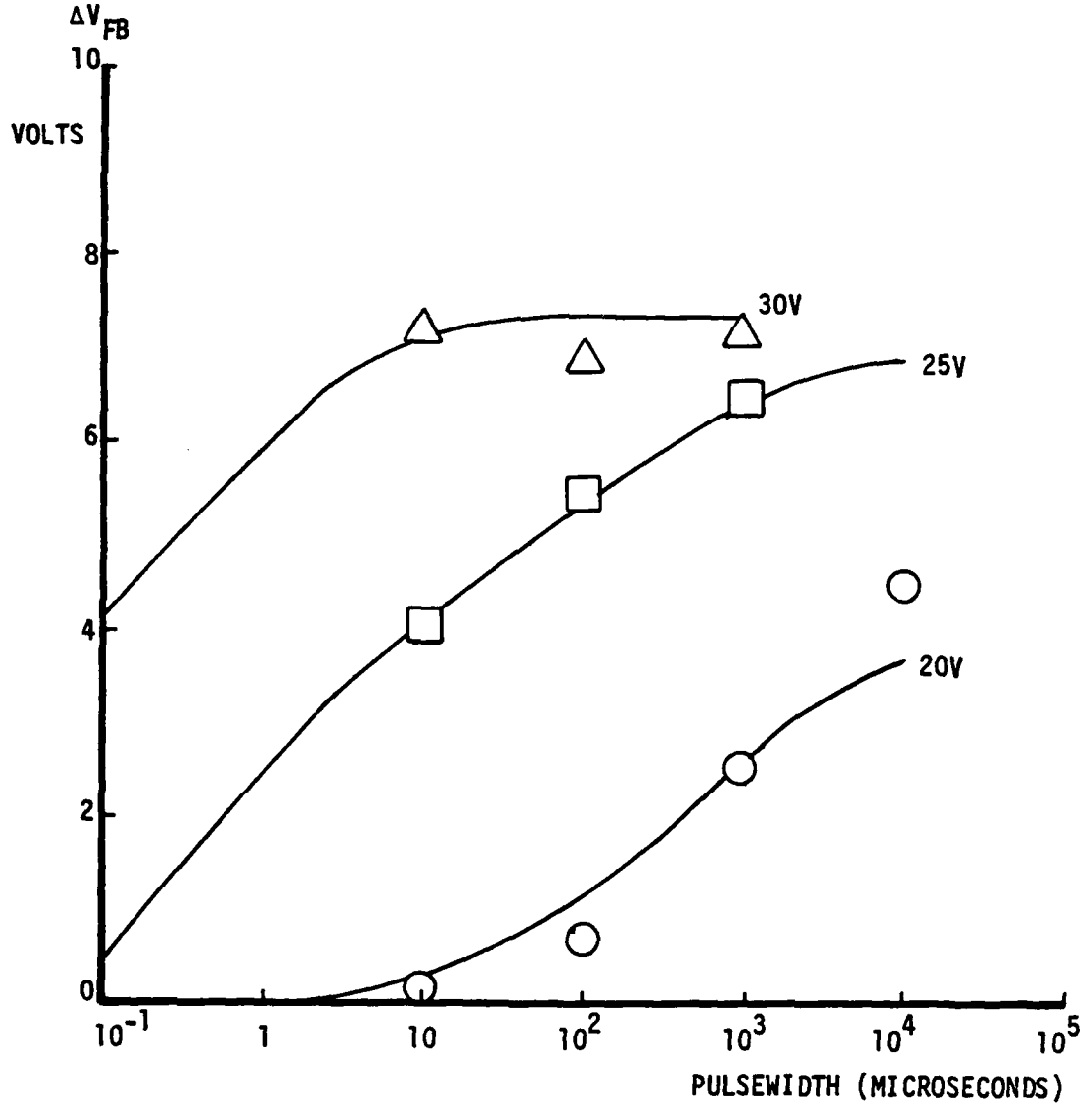


Figure 4-10: Write Characteristics: 1.5 x 10^{15} cm^{-2} Dopant Density.

85 angstrom oxide, 312 angstrom nitride.
Calculated curves. Measured data points (Ref [65]).

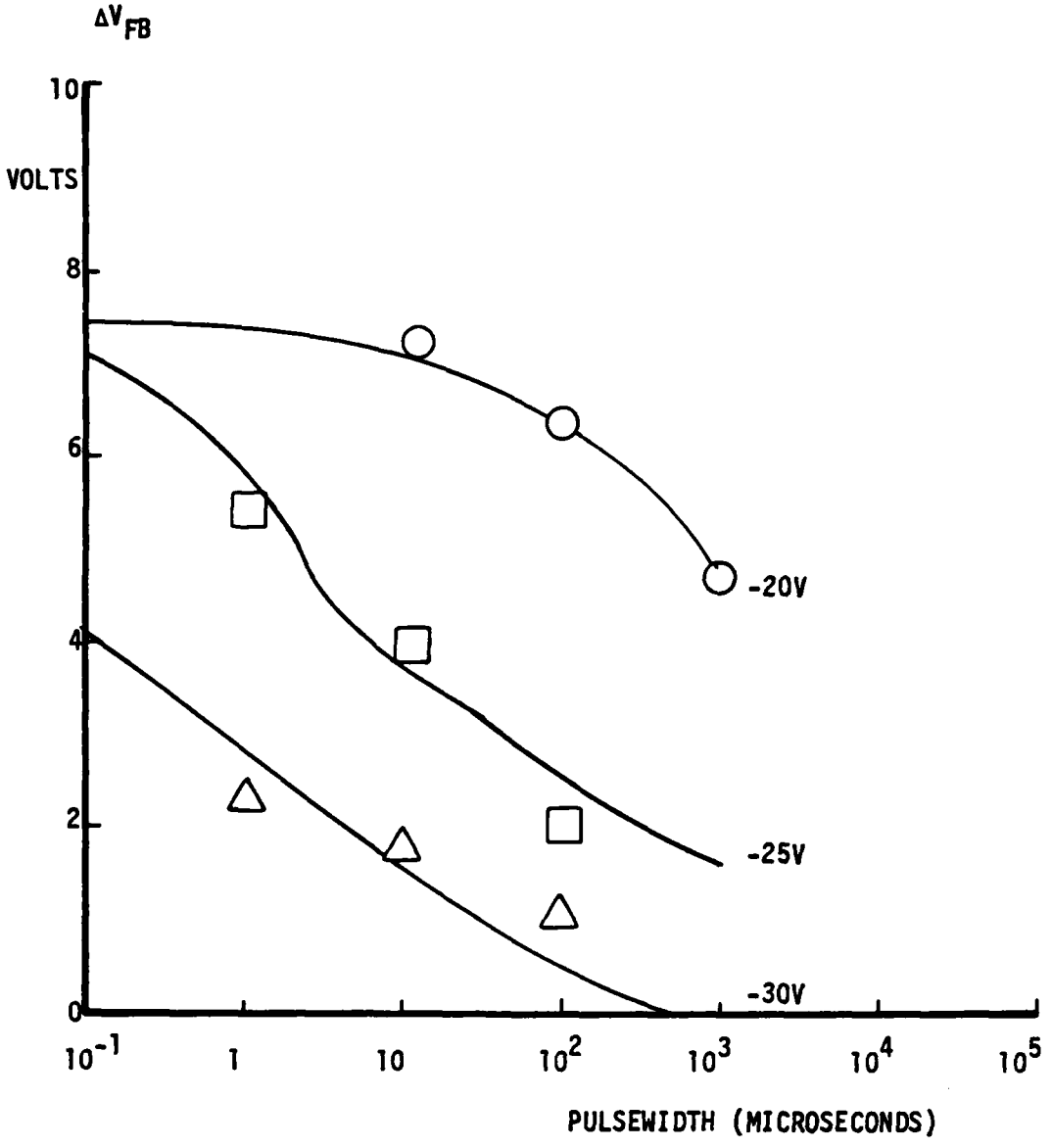


Figure 4-11: Erase Characteristics: 1.5 x 10^{15} cm^{-2} Dopant Density.

85 angstrom oxide, 312 angstrom nitride.
Calculated curves. Measured data points (Ref [65]).

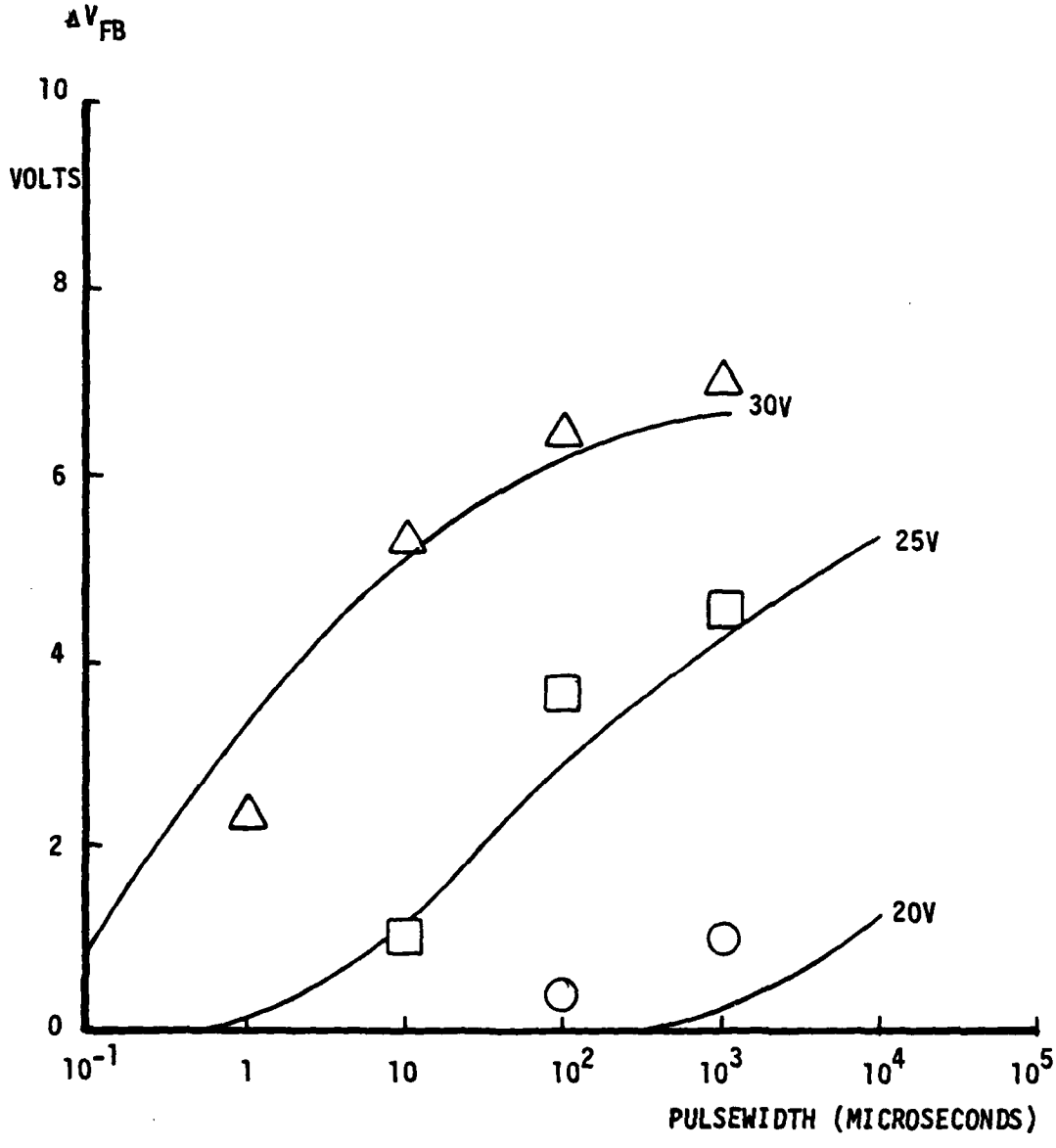


Figure 4-12: Write Characteristics: No Interface Dopant.

85 angstrom oxide, 372 angstrom nitride.
Calculated curves. Measured data points (Ref [65]).

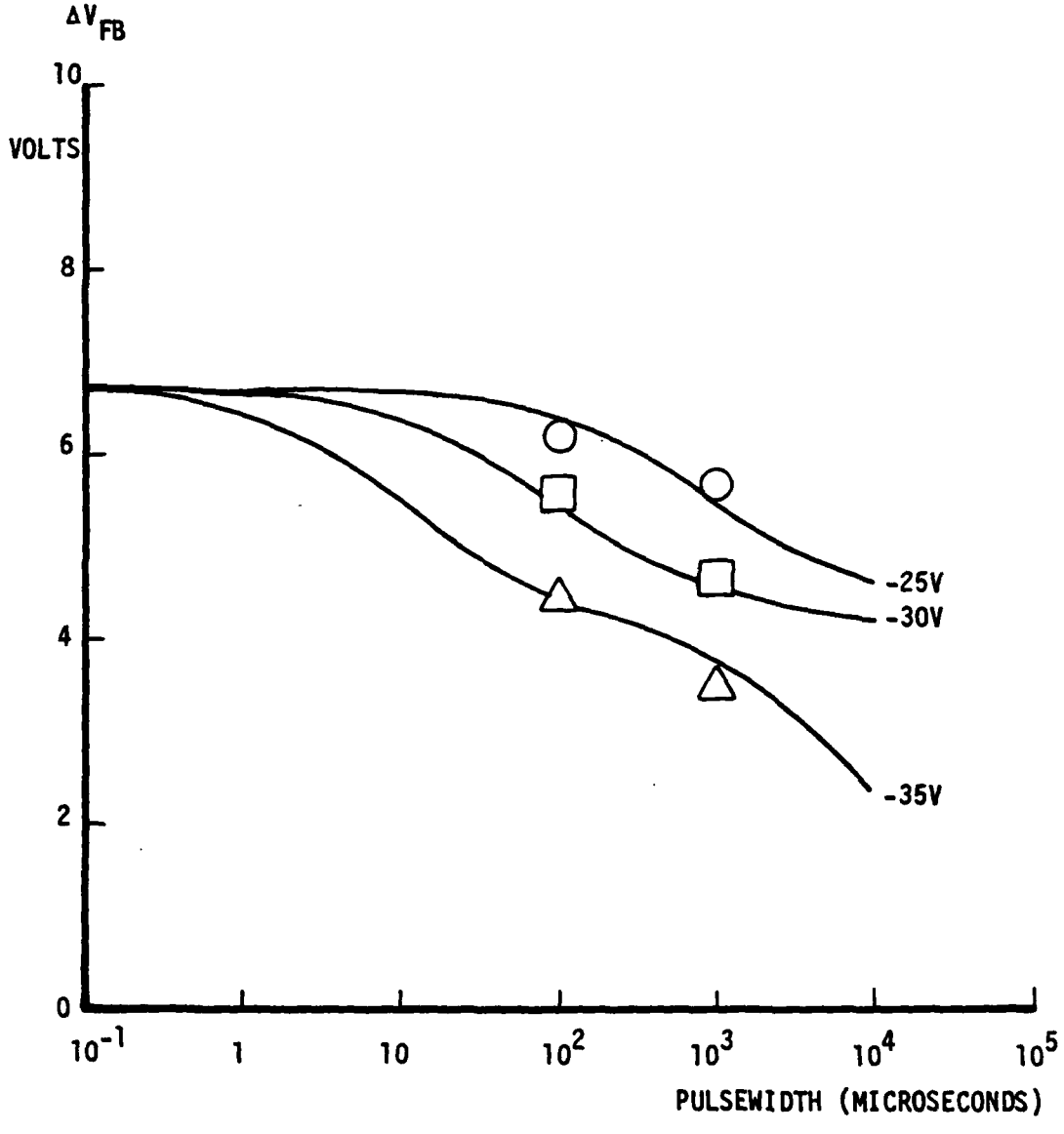


Figure 4-13: Erase Characteristics: No Interface Dopant.

85 angstrom oxide, 372 angstrom nitride.
Calculated curves. Measured data points (Ref [65]).

Physical Parameters			
Dopant Density	1.5×10^{15}	None	cm^{-2}
Oxide Thickness	85	85	angstroms
Nitride Thickness	312	372	angstroms
Capture Cross Section			
Interface Dopant	2.5×10^{-12}	—	cm^{2}
Oxide-Nitride Interface	—	5.0×10^{-14}	cm^{2}
Deep Nitride	1.0×10^{-13}	1.0×10^{-13}	cm^{2}
Shallow Nitride	1.0×10^{-13}	1.0×10^{-13}	cm^{2}
Trap Density			
Interface Dopant	4.5×10^{12}	—	cm^{-2}
Oxide-Nitride Interface	—	1.5×10^{12}	cm^{-2}
Deep Nitride	3.5×10^{18}	3.5×10^{18}	cm^{-3}
Shallow Nitride	2.5×10^{18}	2.5×10^{18}	cm^{-3}
Trap Depth			
Interface Dopant	1.7	—	eV
Oxide-Nitride Interface	--	1.25	eV
Deep Nitride	2.0	2.0	eV
Shallow Nitride	1.35	1.35	eV
Poole-Frenkel Constant	.00029	.00029	$(Vcm)^{1/2}$

Table 4-2: Model Parameters For Write/Erase Characteristics

Observations

The agreement between the measured and calculated write curves for the interface doped MNOS device is very good even for the simple charge injection model used.

The match between the measured and calculated erase curves for the interface doped MNOS device is not as exact as for the write condition. This is in spite of the more complex discharge process of the model. To obtain these results it was necessary to assume that the value of the capture cross section for holes of the interface dopant traps occupied by electrons was of the physical size of the ultrathin film islands. This is not unreasonable because each island stores many electrons and therefore positive hole trapping/recombination is highly enhanced. The ratio of maximum stored charge density (from TSC measurements) to island density is 6×10^{12} charges per square centimeter to 4×10^{9} islands per square centimeter, based on the island size of 1.5×10^{-10} cm^2. Thus a negative charge from up to 1500 electrons would influence the hole trapping at each of the metal dopant sites. It was also necessary to incorporate a reduction of the silicon-silicon oxide valence band barrier from the usual 3.8 eV down to 2.9 eV to predict the interface doped MNOS device erase characteristics. This reduction is explained by the effect of some dopant penetration into the oxide. The dopant inclusion in the oxide would affect the Fowler-Nordheim conduction through the oxide.

The agreement between the measured and calculated write curves for the conventional, no interface dopant, MNOS device is good. The major

difference occurs for the low voltage (20 volt) write curve. This could be attributed to an experimental error during Neugebauer's measurements. Running the model using a write pulse amplitude of 21 volts produced a curve coincident with the reported 20 volt data points.

The model produced erase curves that matched the measured data points for the conventional, no interface dopant, device. This agreement was obtained using the full silicon-silicon oxide valence band barrier energy for holes of 3.8 eV. This tends to reinforce the concept of interface dopant penetration into the oxide as the mechanism which caused the barrier lowering and subsequent enhanced hole conduction in the interface doped structure. The capture cross section for holes of the oxide-nitride interface traps was the same order as for electrons. This is expected because the oxide-nitride interface traps result from the physical mismatch between the oxide and nitride which would produce a uniform distribution of single charge traps over the whole device area. This is a very different mechanism from the metallic island traps resulting from the evaporated tungsten interface dopant.

4.3 Summary

A model of the charging and discharging processes in conventional and interface doped MNOS devices was proposed. Charging was based on electron injection from the silicon conduction band. The discharge process was based on hole injection from the silicon valence band and electron detrapping from the nitride and ejection from the nitride conduction band into the silicon. Using appropriate trap parameters, determined from thermally stimulated current measurements, the model predicts the form of the charge centroid-injected charge relation and

accurately predicts the write/erase characteristics of both conventional and interface doped MNOS structures.

5. CHAPTER FIVE - CONCLUSIONS, LIMITATIONS, RECOMMENDATIONS

Conclusions

The model developed in this dissertation successfully explains the behavior of interface doped MNOS devices observed by Neugebauer and Barnicle.[65] The difference in erase characteristics between the conventional and the interface doped MNOS structure is due to the large, hole capture cross section of the evaporated tungsten dopant traps as compared to the naturally occurring oxide-nitride interface traps and also due to the reduced oxide energy barrier for holes in the interface doped MNOS device. The stability of charge storage in the device up to 250^{o}C is due to trapping in dopant traps which are deeper than 1.7 eV and in bulk nitride deep traps which are deeper than 2 eV. The anomalous increase in threshold voltage upon application of a low negative bias only after performing a high temperature write operation which Neugebauer observed during accelerated retention tests is explained by charge redistribution in the deep dopant and nitride traps.

The model also successfully demonstrated, for interface doped MNOS and conventional MNOS structures, calculated threshold voltage shift versus write/erase pulse amplitude and duration data that matched measured curves, and calculated charge centroid versus injected charge curves that qualitatively matched measured data.

Experimental evidence has been developed that clarifies several concepts relating to charge storage in interface doped MNOS structures. It has provided the first determination of the trapping levels due to

the interface dopant and has provided a comprehensive examination of trapping levels and trapped charge density throughout the MNOS structure. The model of the charging/discharging process in MNOS structures developed in this study was based on these trap parameters.

The charge centroid data conclusively proves that the interface dopant does cause greatly increased trapping at the oxide-nitride interface. Additionally, it shows that charge storage in interface traps does saturate at a stored charge level much below the value of the dopant atomic density (6×10^{12} charges per square centimeter for a 2×10^{15} cm^{-2} dopant atomic density). This leads to considerable bulk nitride trapped charge under high charge injection conditions. The saturation level of the interface traps is a stronger function of the oxide thickness than the evaporated dopant density. The saturation level decreases as the oxide thickness increases. This is due to the influence of the oxide thickness on the oxide electric field which in turn has a strong effect on the injected charge and subsequent trapping and redistribution within the structure.

The thermally stimulated current results have detailed the trap level distribution at the oxide-nitride interface (dopant and naturally occurring interface traps) and in the nitride. With respect to the nitride conduction band edge, interface dopant trap levels were observed at 1.71 - 1.86 eV, naturally occurring oxide-nitride interface trap levels at 0.70 - 0.93 and 1.30 - 1.34 eV, and nitride trap levels at 1.14 - 1.19, 1.35 - 1.58 and 1.92 - 2.32 eV. Detrapped charge densities up to 6×10^{12} cm^{-2} from interface dopant traps, 3×10^{13} cm^{-2} from oxide-nitride interface traps, 1.5×10^{18} cm^{-3} from shallow nitride

traps and 8×10^{18} cm^{-3} from deep nitride traps were observed. The dopant traps and the interface traps have relatively narrow energy ranges and are easily incorporated into a predictive charge/discharge model. However, the wide energy range for the nitride traps makes an a priori selection of trap levels for use in a model questionable.

This study has demonstrated that comparison of TSC spectra from various MIS structures can lead to information on traps in specific parts of a complex multilayer device.

Model Limitations

A definite limitation on the ability of this model to predict endurance performance lies in the fact that the silicon-silicon oxide surface states have not been incorporated into the model. There have been numerous studies which have shown that, with write/erase cycling, the number of surface states increases. It has been proposed that this increase plays a part in the ultimate endurance of an MNOS device. Additionally, others have proposed that the process of passing large numbers of charges through the insulator layers (oxide and nitride) damages these layers, reducing their insulating properties, and causing wear-out. This effect is not represented in the model.

A considerable spread of trap energies in the bulk nitride was observed in this effort. These energy levels can be affected by variations in processing as well as a simple parameter such as nitride thickness. A result of this is that an a priori assumption of nitride energy trap levels in order to use model results to design and fabricate

devices could not be recommended at this time.

Recommendations for Further Work

The success of the TSC and centroid measurement techniques in the investigation of the evaporated tungsten interface doped MNOS structure leads to several interesting extensions of this study.

A cooled substrate could be used during the dopant deposition. This would reduce the thin film "island" size but increase the number of islands. The TSC and centroid techniques could then be used to determine the parameters of this form of structure. If considerably more traps with the same, or even slightly smaller, capture cross section could be produced there could be increased trapping at the interface and reduce the bulk nitride trapping further still.

In their survey of potentially useful interface dopant materials, Neugebauer and Barnicle[65] found several elements that were ineffective in improving the write/erase characteristics of a DMNOS device. It would be interesting to try to examine the interface trap properites introduced by these metals, particularly one like molybdenum which has elemental properites very similar to two successful interface dopants, tungsten and chromium. Are the trap densities less or trap levels shallower?

This study examined a dopant deposited via electron beam evaporation. There would be considerable interest in a study on an ion implanted dopant. Ion implantation opens the door to different dopant

species. It is flexible with respect to locating the dopant in the insulator layer. It offers the potential for inclusion of a dopant induced trap layer in a single layer insulator MIS structure, simplifying fabrication.

Retention and write/erase cycling should be studied using the model. Accurate, long term, retention characteristics are time consuming to measure. Once verified in the retention mode, the model could be used to predict new device retention characteristics using trap parameters ascertained during model calculations of the more easily measured write/erase characteristics. In spite of the anticipated model limitations for total endurance predictions, it would be interesting to observe the "permanent" trapping effects of the bulk nitride deep traps on write/erase characteristics. A separation of bulk nitride storage effects from surface state generation effects on endurance might be possible.

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I. APPENDIX I - DEVICE FABRICATION TECHNIQUES

The techniques used to fabricate the MIS structures used for the TSC measurements are typical of interface doped devices and are described here.

1. The fabrication process started with conventionally cleaned n-type, 5 ohm-cm, (100) orientation silicon substrates. The (100) orientation is selected to minimize the thin oxide induced silicon-silicon oxide interface states.

2. The oxide layers were produced by dry thermal oxidation in a 20 percent oxygen atmosphere with a nitrogen carrier gas at a total flow rate of 2 liters per minute. The temperature was 900°C and the oxidation times were 9 and 60 minutes resulting in nominal ellipsometrically measured oxide thicknesses across a wafer of 35 ± 2 angstroms and 82 ± 2 angstroms respectively. The variations in measured oxide thickness across the wafer are due to the ellipsometer settings uncertainty rather than measurable oxide thickness variations, as verified by repeated measurements for the same spot on a wafer.

It should be noted that for thin oxides, absolute thickness loses its meaning due to the finite silicon-silicon oxide transition region [73, 74, 75], estimated to be from 10 to 50 angstroms. However, ellipsometric techniques are commonly used to determine a thin oxide "thickness" to characterize an MNOS device. For this study a silicon dioxide "thickness" for each thin oxide was calculated via ellipsometric techniques [104] assuming an index of refraction of 1.45, which is typical of silicon dioxide. To verify comparability of these measurements with

data by others, measurements were made of oxides grown by the self limiting, hot nitric acid oxidation of silicon.[105, 106] The ellipsometrically measured thickness was 17 ± 3 angstroms for oxidation times of 15, 25 and 60 minutes as compared to the reported self limiting 18 ± 2 angstrom thickness for an oxidation time range of 8 to 75 minutes. In all cases the silicon wafers underwent a cleaning process, including a final HF etch, immediately prior to being inserted into the oxidation furnace. This insured a consistent pre-oxidation surface condition and therefore a repeatable oxide growth.

3. All the silicon nitride layers were nominally 400 angstroms thick. The nitride was deposited in a 775°C hot-wall tube by the reaction of ammonia (NH_4) and dichlorosilane (SiH_2Cl_2) with a NH_4:SiH_2Cl_2 ratio of 1000:1 in a nitrogen carrier gas. A 75 liter per minute nitrogen flow was used with a 5 liter per minute ammonia flow. The furnace heating elements were adjusted to produce a growth rate of 64 angstroms per minute and a 400 angstrom nitride film uniformity of ±9 angstroms across each wafer of a five wafer boat load.

4. The interface dopant, tungsten, was electron beam evaporated from a water cooled crucible in a 10^{-6} torr vacuum at rates from 3×10^{14} up to 1.2×10^{15} atoms per square centimeter per second. Specific deposition rates were established prior to shutter opening and then the total deposition was monitored by quartz crystal thickness monitors. Depositions were made at 0.25 to 1.0 angstroms/second for tungsten "thicknesses" of 0.5 to 17 angstroms (eleven hertz of crystal monitor frequency change per angstrom of tungsten).

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CHARGE TRAPPING IN INTERFACE DOPED MNOS STRUCTURES.(U)
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The tungsten deposition system was calibrated by Rutherford Backscattering (RBS) analysis[107, 108] of interface doped nitride-oxide-silicon structures fabricated using the same process as for the TSC devices. The RBS analysis used 2 MeV helium ions at both perpendicular and glancing (85^{o} from surface normal) incidence to determine the tungsten atomic concentration and the nitride thickness.[86] The tungsten density determined by RBS analysis is compared in Figure I-1 to an estimate of tungsten atomic concentration made by assuming a film with uniform coverage, deposited tungsten density equal to the bulk density of gold (bulk tungsten is 18.6 to 19.2 gm/cc; bulk gold is 19.3 gm/cc), and identical sticking coefficient for tungsten on the metal covered quartz crystal monitor as on the thin oxide film, for all thicknesses of tungsten up to 200 angstroms. Figure I-1 shows this data as a function of "effective" thickness as determined by the quartz crystal monitor. The error in the estimate at the low tungsten densities is attributed to the shutter opening and closing times becoming comparable to the tungsten deposition time.

The nitride thicknesses determined by the RBS technique were 20 to 45 angstroms thinner than the ellipsometric determinations. This could have been due to the tungsten diffusing into the nitride during the silicon nitride deposition. The likelihood of this diffusion occurred is further reinforced by the observation that the tungsten RBS peaks were significantly broadened. This broadening is a characteristic of a layer of material with a diffuse rather than a sharp spatial profile.

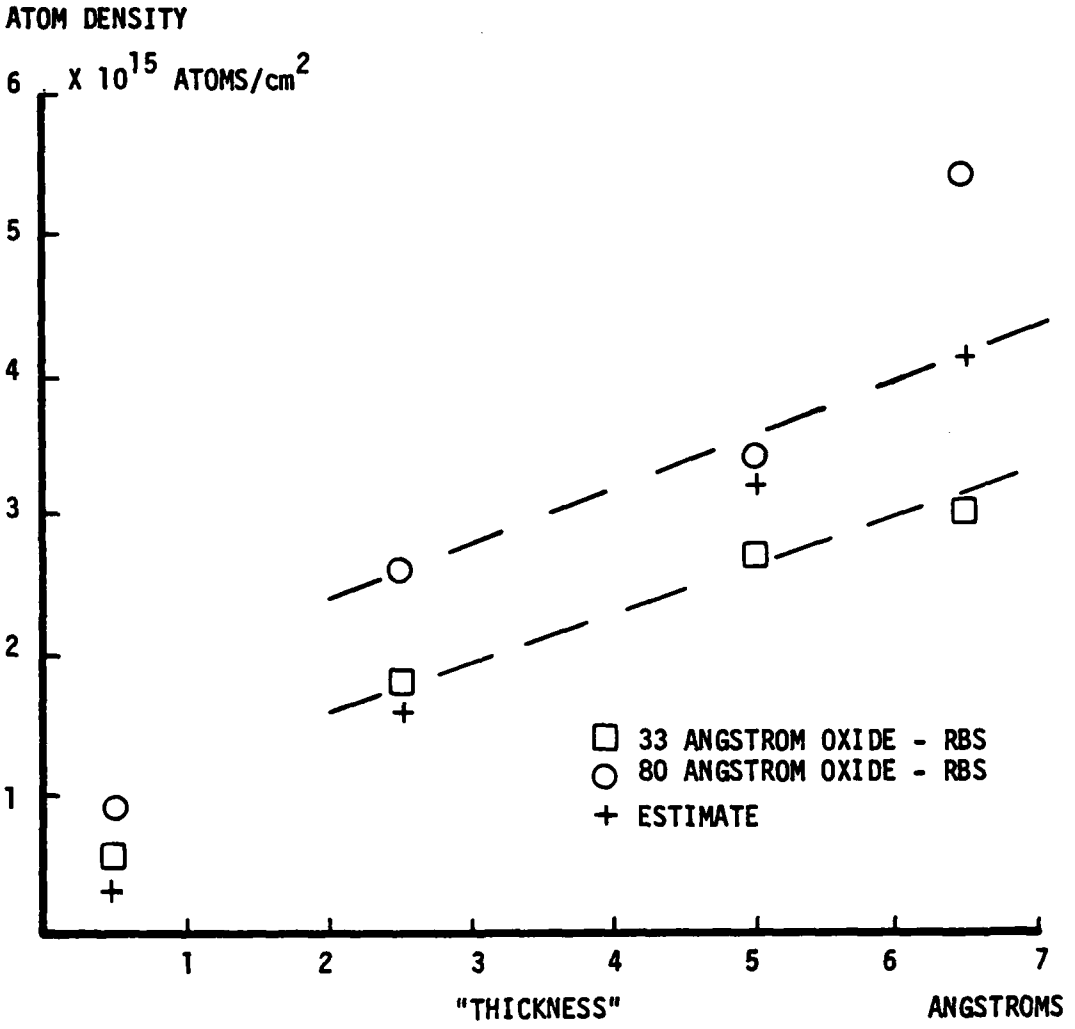

Figure I-1: Tungsten Atomic Concentration vs Effective Thickness

II. APPENDIX II - CHARGE CENTROID DATA ACQUISITION PROCEDURES

Referring to Figure 2-11:

1. Open feedback loop at Switch 2; determine device capacitance via LIA; select R and C_I values; adjust LIA output offset for zero dc output; start calculator program to accept data input; set write pulse amplitude and duration; reset feedback integrator with Switch 3 and then set for "V Run"; reset charge integrator with Switch 1 and leave in "Q Reset".

2. Set charge integrator switch to "Q Run"; start X-Y recorder and multichannel scanner A/D converter; allow 10 to 20 scanner samples/channel to collect data for charge integrator bias current adjustment; initiate write pulse (time t_1 in Figure 2-12).

3. Verify write by observing Q/C trace on X-Y recorder; close feedback loop with Switch 2 (time t_2 in Figure 2-12);observe V_{FB} effect.

4. Stop scanner to stop run.

VITA

William Gardner Sutton was born 8 January 1944 in Boston, Massachusetts. He attended public schools in Natick, Massachusetts; Takoma Park, Maryland; Hicksville, New York and Silver Spring, Maryland. In June 1961 he graduated from Montgomery Blair High School. He enrolled at Syracuse University in 1961 and graduated Summa Cum Laude in June 1965 with a Bachelor of Science in Electrical Engineering. He was elected to the Tau Beta Pi and Eta Kappa Nu Honor Societies. Designated a Distinguished ROTC Graduate, he was commissioned in the USAF. In September 1965 he entered Case Institute of Technology. He was awarded a Master of Science in Electrical Engineering in August 1968 from Case-Western Reserve University. He reported for active duty in August 1968. His career includes assignments as a Project Engineer in the Ground Electronics Engineering Installation Agency (GEEIA) at Griffiss AFB, NY; in Hq AFCS at Richards-Gebaur AFB, MO and in the DoD Electromagnetic Compatibility Analysis Center (ECAC) at Annapolis, MD. In January 1974 he entered the PhD program of the School of Engineering, Air Force Institute of Technology. In October 1975 he was assigned to the Air Force Avionics Laboratory to complete his research program.


DATE
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